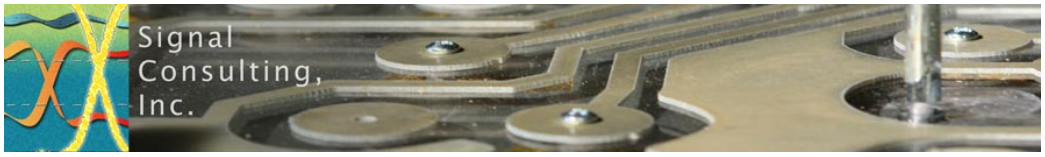
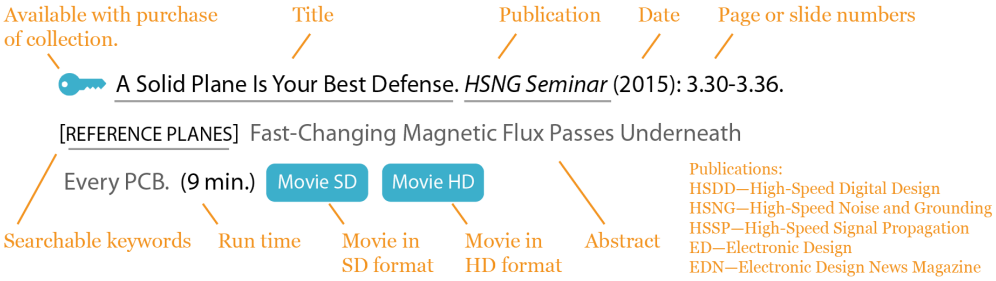


Title Index



10 Reasons Why I Love the BGA. ED (3/17/1997).
[CHIP PACKAGING] Ball Grid Array (BGA) packages are taking the industry by storm, and I'm glad to see it.

2-D Quasistatic Field Solver. EDN (9/27/2001).
[SIMULATION, TEM MODE] If your system violates any of these assumptions, the simulator produces wrong answers.

A Solid Plane Is Your Best Defense. HSNG Seminar (2015): 3.30-3.36.
[CROSSTALK, REFERENCE PLANES] Your Reference Plane Is Not Perfect. Fast-Changing Magnetic Flux Passes Underneath Every PCB. (9 min.) Movie SD Movie HD

A Time for All Things. EDN (6/21/2001).
[CHIP PACKAGING, DIFFERENTIAL SIGNALING, GROUND BOUNCE] There is a good time and a bad time for a chip to sample its digital inputs.

A transmission line is always a transmission line. EDN (4/4/2002).
[CHARACTERISTIC IMPEDANCE, REFLECTIONS, TRANSMISSION LINE] Does the input impedance behave one way on a long transmission line but differently when the load is adjacent to the driver? How does it know what to do?

AC Coupling Layout (for XAUI 3.125 Gb/s). Newsletter v10_02 (5/18/2007).
[DATA CODING, LAYOUT, REFLECTIONS] The parasitic body capacitance of the AC coupling caps perturbs the characteristic impedance of your transmission line.

AC Terminators. Newsletter v2-24 (9/9/1998).
[POWER DISSIPATION, TERMINATION] The promise of an AC terminator is the idea that maybe, just maybe, there is a value of C big enough to make a good termination, but at the same time small enough to not draw much current from the source.

Acceptable Crosstalk. Newsletter v5-11 (10/30/2002).
[CROSSTALK] What is the limit of crosstalk that can be ignored? (and frozen turkeys)

Acceptable Failure. EDN (3/2/2000).
[METASTABILITY] Without clearly quantified limits on the "acceptable probability of failure," you never know whether you have implemented too little or too much of your favorite failure-rate cure.

Accurate Series Termination. Newsletter v4-14 (11/1/2001).
[TERMINATION] How are you supposed to calculate an appropriate series termination when you have such a large variance in the source impedance of the driver?

ADC grounding. EDN (12/7/2000).
[GROUNDING] Chip designers often internally partition the ground-reference net (or substrate) for an ADC into isolated analog and digital regions.

Adequate Bandwidth. Newsletter v11_03 (5/19/2008).
[BANDWIDTH, PROBES, TESTING] A bandwidth-limit feature performs a service somewhat like vertical averaging, in that it reduces random noise, but it does not require a repetitive signal.

All About Surface-Mount Ferrites. Lee Hill. EDN (8/21/2008).
[EMC, FERRITE BEADS] Don’t use a ferrite bead unless you have data showing impedance versus frequency while under the influence of DC bias current, and don’t operate ferrite beads close to their maximum rated current.

Analog Equalizer Examples. HSSP Seminar (2015): 3.50-3.54.
[EQUALIZATION, EXAMPLES] Analog 1-Pole Equalization Circuit. Refinement for Constant-Impedance Input. Symmetric Equalizer. Balanced, Constant-Impedance Symmetric Equalizer.

Analog to Digital Conversion Parameters. Newsletter v9_03 (2/22/2006).
[SAMPLED DATA, TESTING] Definitions of A/D specification terms, with hints about "specsmanship" in these numbers

Another Version of a Coax Probe. Newsletter v1-18 (11/26/1997).
[PROBES] What kind of probes do I need for looking at noise (<100 mV to 300 mV range) on the various ground pins of some gigabit transceivers?

Approaching the Edge. DesignCon 2004 (2/1/2004).
[MANAGEMENT, PROBES] Worst-case budgets don’t work if you don’t include all the necessary factors, or if you make wrong assumptions to fill in gaps in the available data.

Arrays of Capacitors. HSDD Seminar (2015): 8.20-8.26.
[BYPASS CAPACITORS, POWER SYSTEMS] Modeling a Complete Power System. Dual-Value Capacitor Arrays. Choose the Smallest Package and the Biggest Value. (21 min.) Movie SD Movie HD

Ask For It. EDN (7/6/2000).
[RISE TIME] A limitation on the minimum rise and fall times is absolutely critical to proper functioning of digital hardware.

Asymmetric Noise Margins. EDN (3/15/2001).
[GROUND BOUNCE, LEVEL TRANSLATION, RISE TIME] Extreme asymmetries in the noise margin budget for a logic family create a preferred logic level.

Asymmetry in Broadside Configuration. EDN (11/14/2002).
[DIFFERENTIAL SIGNALING, LAYER STACK, LAYOUT, SKEW] In general I avoid broadside-coupled traces unless they are made necessary by routing considerations.

Audio-Frequency Isolation. HSNG Seminar (2015): 4.23.
[CROSSTALK, EXAMPLES, MIXED SIGNALS, SILAB HSNG] Mixed-Signal Isolation, Part I, "Audio Examples".

Crosstalk at audio frequencies. Mitigation strategies. (15 min.) Movie SD Movie HD

Aunt Judy. EDN (11/8/2007).
[MANAGEMENT] Old Aunt Judy approaches you at a reception, with a little halt in her voice, and says, "You know about electronics, right? Well, I've got this old 8-track tape player…

Backplane Design. EDN (5/25/2000).
[BACK PLANE, DIFFERENTIAL SIGNALING, LAYER STACK, SERIAL LINK] Differential trace geometry, power and ground stackup for big backplane.

Benefits of Resistive Probe. Newsletter v5-4 (3/11/2002).
[PROBES] Here are ten good reasons to consider using a resistive-input probe.

BGA Crosstalk. Newsletter v8_03 (3/1/2005).
[CROSSTALK, GROUND BOUNCE] Details, measured lab results, and theory of crosstalk involving hundreds of outputs switching simultaneously in a high-speed Xilinx Virtex-4 FPGA package, as delivered to the Xilinx tech on-line forum March 1, 2005.

BGA Ground Ball Placement. HSNG Seminar (2015): 2.26-2.76.
[CHIP PACKAGING, CROSSTALK, GROUND BOUNCE, SILAB HSNG] Measurement of BGA ball inductance. Effect of layout on measured values. Implication for ball pinouts. (35 min.) Movie SD Movie HD

BGA Package Examples. HSDD Seminar (2015): 2.18-2.21.
[CHIP PACKAGING] Plastic Ball Grid Array (PBGA). Flip-Chip. Upside-down with heat spreader.

Bi-directional Alternatives. Newsletter v3-3 (1/22/1999).
[CIRCUIT TOPOLOGY, MULTI DROP, PCI] Hanging four loads on a bi-directional line; how PCI "reflected wave switching" works

Bi-directional Termination. HSDD Seminar (2015): 6.60.
[CIRCUIT TOPOLOGY, MULTI DROP, TERMINATION] A uni-linear structure that can reverse direction. (4 min.) Movie SD Movie HD

Bi-directional Terminations. Newsletter v2-20 (8/6/1998).
[CIRCUIT TOPOLOGY, MULTI DROP, TERMINATION] Using a series terminator at both ends of the line.

Big Buffer. Newsletter v8_07 (10/18/2005).
[CROSSTALK, GROUND BOUNCE] Do you suppose there is much SSO noise margin left in a typical IC package design? Can you safely exceed the loading guidelines without causing SSO errors? I doubt it.

Big Hurl. EDN (7/21/2005).
[MANAGEMENT, POWER SYSTEMS, TRANSMISSION LINE] Engineers enjoy a long tradition of experience with dynamic processes. We have developed over the centuries many diverse means of dealing with them.

Blocking Capacitor Performance. EDN (4/5/2012).
[LEVEL TRANSLATION, REFLECTIONS, SERIAL LINK] Cut a small round void in the reference plane layer right under the capacitor, thus relieving the capacitance to ground, while at the same time slightly increasing the series inductance.

Body and Soul. EDN (11/27/2012).
[MANAGEMENT] Even if you never master a musical instrument to the point of performing onstage, the simple act of learning to play music stimulates parts of your brain critical to creativity and insight.

Both-ends Termination. HSDD Seminar (2015): 6.28.

[CIRCUIT TOPOLOGY, TERMINATION] The Ax-Murderer Approach to Termination. (10 min.)
Movie SD Movie HD

Both-ends Termination. EDN (1/18/2001).
[TERMINATION] The both-ends termination is supremely tolerant of imperfections within the transmission system and within the terminators themselves.

Breaking Up a Pair. HSSP Seminar (2015): 6.32-6.33.
[LAYOUT, REFLECTIONS, TRANSMISSION LINE] Excess Inductance Method of Analysis. (6 min.)
Movie SD Movie HD

Breaking Up a Pair. EDN (11/9/2000).
[LAYOUT, REFLECTIONS, STRIPLINE] The two traces comprising a differential pair, when routed close together, share a certain amount of cross-coupling. This coupling lowers the differential impedance between the traces.

Building a Signal Integrity Department. EDN (6/4/1998).
[MANAGEMENT] What sort of a mission do you give to a department of signal integrity?

Bus Architecture and Timing. DesignCon 1999 (1/30/1999).
[BACK PLANE, MULTI DROP, RINGING] The ratio (bus delay)/(clock period) is a key indicator of bus design difficulty.

Buying Time. EDN (5/2/2002).
[DIFFERENTIAL SIGNALING, SKEW] Two strategies for minimizing the intra-pair skew accumulated by a differential net: (1) A pair that starts and ends going north has by definition equal numbers of right and left-hand turns. (2) How your layout enters or leaves a BGA makes a difference.

Bypass Capacitor Array. Newsletter v6-02 (1/24/2003).
[BYPASS CAPACITORS, POWER SYSTEMS] This spreadsheet produces a beautiful color version of my figure 8.9 showing the impedance of each element of a power system and also the composite impedance of all four elements taken in parallel.

Bypass Arrays. Newsletter v1-6 (7/25/1997).
[BYPASS CAPACITORS, LAYOUT] Does anyone out there actually DESIGN their bypassing networks?

Bypass Capacitor Layout. Newsletter v2-3 (1/23/1998).
[BYPASS CAPACITORS, LAYOUT] Little traces between your bypass capacitors and the power planes have a big effect on performance.

Bypass Capacitor Layout. PCD (8/1/1997).
[BYPASS CAPACITORS, LAYOUT, POWER SYSTEMS] The primary symptoms of an inadequate, old-fashioned bypass capacitor array are increased power supply noise, increased crosstalk among signal traces, and increased electro-magnetic radiation.

Bypass Capacitor Sequencing. Newsletter 9_07 (10/4/2006).
[BYPASS CAPACITORS, LAYOUT] A trace of any practical length placed in series with the power terminal of a high-speed IC (especially one with multiple VCC pins) radically increases power supply noise at the VCC terminal and should be avoided like the plague.

Bypass Multi-Valued Arrays. Newsletter v1-17 (11/14/1997).
[BYPASS CAPACITORS, POWER SYSTEMS] I discourage engineers from combining together different-valued capacitors if they share the same package format.

Cable Shield Grounding. Newsletter v2-2 (1/16/1998).
[CABLES, CONNECTORS, EMC, GROUNDING] Joe, I am going to disagree with your suggestion that a shield with a resistor at one end acts as an effective EMI shield. In high-speed digital applications, it doesn't.

Capacitance. HSNG Seminar (2015): 1.21-1.30.
[CAPACITANCE, EXAMPLES] Current Flows in Loops. Return Path for an Antenna. Measuring Capacitance. Handheld Capacitance Meter. Example: Capacitance of Scope Chassis to Earth. Approximate Values of Capacitance. (14 min.) Movie SD Movie HD

Capacitive Loading of Transmission Line. HSDD Seminar (2015): 4.31-4.34.
[CAPACITANCE, CIRCUIT TOPOLOGY, RINGING, TRANSMISSION LINE] Tuned circuit analogy helps explain resonance.

Capacitor Layout Matters. EDN (9/5/2002).
[BYPASS CAPACITORS, LAYOUT, POWER SYSTEMS] Your problem is likely caused by the layout, which has more than tripled the inductance of each bypass capacitor, not the values of types of capacitance.

Capacitor Placement. Newsletter v2-1 (1/7/1998).
[BYPASS CAPACITORS, LAYOUT] The function of a bypass capacitor is this: to help returning signal current get from the board back into the driver.

Carrier Detection. EDN (9/4/2003).
[ATTENUATION, SERIAL LINK] What happens when the opposing end of a link is disconnected, powered down, or disabled.

Changing Reference Planes. HSSP Seminar (2015): 6.36-6.38.
[LAYER STACK, REFERENCE PLANES] Differential U-Turn. Purpose of Ground Connections Between the Planes. (9 min.) Movie SD Movie HD

Characteristic Impedance. HSDD Seminar (2015): 4.4-4.7.
[CHARACTERISTIC IMPEDANCE, TRANSMISSION LINE] Response to Step Input. Ice-Cube Tray Analogy. Equivalence of Z0 and RTERM. (15 min.) Movie SD Movie HD

Characteristic Impedance of Lossy Line. EDN (10/3/2002).
[CHARACTERISTIC IMPEDANCE, DIELECTRIC LOSS, SKIN EFFECT] Skin-effect losses increase the real part of the impedance curve in the vicinity of the skin-effect onset, while the dielectric losses decrease the real part of impedance in the same area.

Charge Arrested. Newsletter v14_03 (4/21/2011).
[EE BASICS, TRANSMISSION LINE] Animations showing the behavior of moving charged particles at an open-circuited transmission-line endpoint.

Charge in Motion. Newsletter v14_02 (4/3/2011).
[EE BASICS, TRANSMISSION LINE] The slight compressibility of the sea of electrons in a metallic conductor generates most high-speed digital design effects.

Charge Unleashed. Newsletter v14_04 (8/10/2011).
[EE BASICS, TRANSMISSION LINE] Charge carriers within a metallic conductor move under the influence of local electrical fields. Lacking any impetus to move; they remain still.

Chip Scale Transmission Lines. Newsletter v7_01 (1/29/2004).
[RINGING, TERMINATION, TRANSMISSION LINE] On-chip interconnections rarely require termination, but pcb traces often do. This conclusion is directly related to the properties of RC and LC transmission lines.

Clean Power. EDN (8/3/2000).
[POWER SYSTEMS] With electromagnetic noise present, you can talk sensibly about potential differences only between points that are co-located, that is, points so close that the total field strength between those points is negligible.

Clock Jitter Propagation. EDN (2/6/2003).
[CLOCKS, JITTER] Any sort of resonance, even a tiny one, spells disaster for a highly cascaded

system.

Clock Modulation. HSNG Seminar (2015): 5.90-5.94.
[CLOCKS, EMC, JITTER] Modulation vs. Scrambling. (6 min.) Movie SD Movie HD

Common and Differential Modes. HSNG Seminar (2015): 5.16-5.23.
[DIFFERENTIAL SIGNALING, EXAMPLES] Differential Example. Every Signal Comprises Two Parts. Why We Care About Modes. UTP Applications Require Extreme Common-mode Attenuation. Imbalanced Output Circuit. Example: Fast/Gigabit Ethernet Launch. (9 min.) Movie SD Movie HD

Common-Impedance Coupling. HSNG Seminar (2015): 1.11-1.20.
[CROSSTALK, EE BASICS, MIXED SIGNALS] PCB Ground Plane Resistance. Slots in the Ground Plane Control the Flow of Audio-Frequency Current. Can a CPU Draw Audio-Frequency Currents?. Example of Entangled System. (28 min.) Movie SD Movie HD

Common Mode Analysis of Skew. EDN (1/22/2004).
[DIFFERENTIAL SIGNALING, EMC, SKEW] A twenty-percent skew creates a ten-percent common-mode component.

Common-mode ground currents. Newsletter v7_02 (3/24/2004).
[GROUNDING] Instead of thinking of your digital ground region as a solid sheet, think of it as a picture frame. This simple model explains the basis of single-point grounding and many other common-mode noise issues.

Comparing Transmission Media. Newsletter v12_05 (7/26/2009).
[ATTENUATION, TRANSMISSION LINE] Transmission line comparisons may be complicated by various geometrical factors, but if you just remember that BIGGER conductors have LESS resistive loss you will have gone a long way towards understanding transmission line losses.

Comparison of Termination Styles. HSDD Seminar (2015): 6.29-6.41.
[CIRCUIT TOPOLOGY, EXAMPLES, TERMINATION] End Termination. Series Termination. AC Termination. Transmission Line States. Dynamic Termination. Proper Design of AC Termination. Power Dissipation. Comparison of Terminations (chart). (39 min.) Movie SD Movie HD

Confirm the Diagnosis. Newsletter v11_02 (3/26/2008).
[CONNECTORS, PROBES, TESTING] The confirmation step is crucial because it takes a lot of time to do re-work, or re-layout, and you must be sure of your conclusions (3.125 Gb/s serial link).

Connecting layers. HSSP Seminar (2015): 5.42-5.43.
[CROSSTALK, REFLECTIONS, VIAS] How Vias Behave as Connectors. (5 min.) Movie SD Movie HD

Connecting Layers. EDN (7/22/2004).
[CONNECTORS, CROSSTALK, LAYER STACK, VIAS] In a multi-layer pcb the vias perform the role of a tiny connector, where the signal-to-ground-via ratio controls via crosstalk.

Connector Examples. HSNG Seminar (2015): 6.12.
[CROSSTALK, EXAMPLES, MIXED SIGNALS, SILAB HSNG] Mixed-Signal Isolation: Parts II-III, "RF Connectors" and "Achieving 120 dB Isolation": Showing the importance of a good ground attachment between the connector and your PCB. (20 min.) Movie SD Movie HD

Connector Mechanical Considerations. HSNG Seminar (2015): 6.13-6.25.
[CONNECTORS] Vibration, shock, salt fog, dust and sand. Trends in interconnect design..

Connectors. HSNG Seminar (2015): 6.1-6.12.
[COAXIAL, CONNECTORS, CROSSTALK, SHIELDING] ERmetZD. Ground Transfer Impedance. Mutual Inductive Noise Coupling. Coaxial Shield Grounding. Ground Transfer Impedance. Examples. Ground Transfer Impedance Calculation. (12 min.) Movie SD Movie HD

Constant-Resistance Termination. EDN (6/12/2003).
[REFLECTIONS, TERMINATION] The constant-resistance circuit forms an almost ideal termination regardless of the input capacitance of the receiver.

Constant-Resistance Equalizer. EDN (7/10/2003).
[EQUALIZATION, REFLECTIONS, TERMINATION] This circuit combines a good termination with a useful equalizing function.

Crossing the River. Doug Smith. EDN (7/24/2008).
[RETURNING SIGNAL CURRENT, RISE TIME, SPLIT PLANES] Cross a river without a bridge and your clothes get soaked. Cross a split-plane gap with a high-speed signal and your whole development schedule gets soaked.

Crosstalk. HSNG Seminar (2015): 1.57-1.88.
[CROSSTALK] Level of Acceptable Crosstalk. Effect of Limited Package Bandwidth. Five Ways to Reduce Crosstalk:. Shrink the Aggressor. Reduce the Coupling. Change the Timing. Improve the Receiver Margins. Reduce the Number of Simultaneous Aggressors. Crosstalk is Highly Directional. (53 min.) Movie SD Movie HD

Crosstalk - Differential Vias. Newsletter v8_02 (2/15/2005).
[CROSSTALK, VIAS] My CAD tools predict the level of crosstalk from differential digital traces to differential analog traces. That's fine, but how about the crosstalk from differential digital vias to differential analog vias? How does that work and how big is it?

Crosstalk - Differential Vias with Grounds. EDN (4/28/2005).
[CROSSTALK, VIAS] Ground vias, used in conjunction with a differential pair, arrest the spread of crosstalk.

Crosstalk - Via to Trace. Newsletter v8_01 (1/25/2005).
[CROSSTALK, VIAS] Measurements of crosstalk between an interplane via and an inner-layer trace relevant to the question of minimum separation between a sensitive differential analog pair and a digital via on the same PCB.

Crosstalk and SSO Noise. Newsletter v3-9 (3/30/1999).
[CROSSTALK, GROUND BOUNCE] What you need is a simple experiment that will separate the effects of SSN (simultaneous switching noise) from other crosstalk.

Crosstalk at Right Angles. Newsletter v3-6 (2/26/1999).
[CROSSTALK, LAYOUT] Crosstalk for traces crossing at right angles.

Crosstalk Experiments. HSNG Seminar (2015): 3.29.
[CROSSTALK, TESTING] Crosstalk Over a Solid Plane. Measuring Tiny Amounts of Crosstalk. Three Ways to Control Unwanted Current. Example: Common-Mode Choke. Example: Current Shunt. Example: Change the Circuit Topology. (34 min.) Movie SD Movie HD

Crosstalk is Directional. HSDD Seminar (2015): 5.21-5.23.
[CROSSTALK, MICROSTRIP, STRIPLINE, TRANSMISSION LINE] Classroom demonstration. (10 min.)
Movie SD Movie HD

Crosstalk NEXT and FEXT examples. HSDD Seminar (2015): 5.55-5.66.
[CROSSTALK, EXAMPLES] Measuring NEXT and FEXT. Effect of trace length, height, and separation. Stripline FEXT. Effect of terminations..

Current-Source Driver. Newsletter v12_04 (4/15/2009).
[BACK PLANE, TRANSMISSION LINE] A current-source driver overlaps its own signal on top of other signals passing by without inhibiting their progress.

(The) Curse of FAST Logic. ED (5/1/1996).

[POWER DISSIPATION, RISE TIME] Your circuits fill a motherboard, not a whole room, but still fall prey to the same signal propagation difficulties encountered in 1946 by Mauchly and Eckert on the ENIAC project.

Daisy-Chain Distribution. HSSP Seminar (2015): 12.35-12.45.
[MULTI DROP] Example: Reflection Amplitude in Daisy Chain. Reflection Coefficient. Reducing the Impact of Tap Capacitance. Daisy-Chain Case Study. Using Five Loads of 3 pF Each. Squeeze Loads Closer Together. Why Overshoot Occurs. Change End Termination to 36 Ohms. Rules for Good Daisy-Chaining. Ironing Out the Bumps (2-in. Spacing). (24 min.) Movie SD Movie HD

Dangerous Games. EDN (4/9/2009).
[MANAGEMENT] You were the kid popping wheelies, probing the limits of unstable equilibrium. On the playground swing set, every jump tested your knowledge of gravity, the nature of inelastic collisions, and bruised ankles.

Dangling Vias. HSSP Seminar (2015): 5.64-5.73.
[LAYOUT, REFLECTIONS, VIAS] Effect on Circuit Performance. Ways to Truncate Dangling Vias. Efficacy of Counter Boring. Wine-Glass Via. Oval Clearances. Differential Via with Oval Clearance. Differential Via with Extra Ground Vias. (31 min.) Movie SD Movie HD

Data Coding for Low Noise. EDN (6/24/2004).
[DATA CODING, GROUND BOUNCE] Limited-weight codes provide noise-canceling properties similar to differential signaling, but using fewer interconnections.

DC Blocking Capacitor Layout. HSSP Seminar (2015): 6.54-6.55.
[DC BLOCK, LAYOUT] General procedure for optimizing the layout. (10 min.) Movie SD Movie HD

DC Blocking Capacitor Placement. Newsletter v7_08 (12/12/2004).
[DATA CODING, LEVEL TRANSLATION, REFLECTIONS, SERIAL LINK] Slower systems sometimes benefit from placing the DC blocking capacitors close to the source, but not multi-gigabit systems.

DC Blocking Capacitor Reflections. HSSP Seminar (2015): 6.56-6.57.
[DC BLOCK, REFLECTIONS] Method of analysis. Example values.

DC Blocking Capacitor Resonance. HSSP Seminar (2015): 6.58-6.61.
[DC BLOCK, LAYOUT] Tuning the cap value doesn't help.

DC Blocking Capacitor Value. Newsletter v7_09 (1/10/2005).
[DATA CODING, LEVEL TRANSLATION, REFLECTIONS, SERIAL LINK] How do I choose the value for a DC blocking capacitor in a serial link application?

DC Loading. Newsletter v11_04 (7/18/2008).
[PROBES, TESTING] This the first case I can recall of a transceiver whose output gets bigger when loaded. Not all LVDS outputs do this.

Debugging Hardware. EDN (8/16/2001).
[TESTING] Debugging new hardware can be difficult and trying. The most common mistakes that most new engineers make when first debugging a system are: trying to debug too much at once, not testing their assumptions, and keeping inadequate records.

Debugging SSO. HSNG Seminar (2015): 2.83-2.86.
[CROSSTALK, GROUND BOUNCE, TESTING] Disrupting the flow of current with cuts and shorts. (7 min.) Movie SD Movie HD

De-constructing Gain and Impedance from S11. EDN (11/10/2005).
[ATTENUATION, S-PARAMETERS, TESTING] From measurements of S11, determine both the gain and characteristic impedance of a uniform transmission structure.

Delay Through Via. Newsletter v2-29 (10/29/1998).
[DELAY, VIAS] For vias which traverse several planes, the delay is a function not only of the via but also of the position and configuration of nearby bypass capacitors.

Design Examples. HSSP Seminar (2015): 5.1-5.15.
[ATTENUATION, EXAMPLES, MICROSTRIP, STRIPLINE] Microstrip Examples. Stripline Examples. Resistive Loss Versus Trace Width. Nickel Plating. Passivation and Soldermask. Effect of Thin Soldermask Coating. Form of Specification for Laminates. Laminate Examples. How Far Can I Go?. Example: PCI Express 2.5 Gb/s. Example: RocketIO at 6.25 Gb/s. (25 min.) Movie SD Movie HD

Designing a Split Termination. EDN (4/3/2008).
[TERMINATION] A Thevenin equivalent circuit helps you understand the need for two resistor values and how they work together to meet the impedance and current-drive constraints imposed by your driver.

Diagnostic Testing (and Tasting). EDN (4/26/2007).
[MANAGEMENT, TESTING] Diagnostic testing requires a keen awareness of all aspects of the system at hand. The operator must remain ever vigilant during testing, aware of even the tiniest clue about system behavior.

Dielectric Effects. HSSP Seminar (2015): 2.31-2.37.
[ATTENUATION, DELAY, TRANSMISSION LINE] Microwaves Heat All Insulating Materials. Measurement of Dielectric Loss. Conduction Current and Displacement Current. Deterioration in Dielectric Constant. Complete Capacitance Model. Approximate Rule of Dielectric Mixtures. (17 min.)
Movie SD Movie HD

Dielectric Loss Tangents. Newsletter v4-5 (6/11/2001).
[ATTENUATION, DIELECTRIC LOSS] For a capacitor formed from a lossy dielectric material, the loss tangent is the ratio at any particular frequency between the real and imaginary parts of the impedance of the capacitor.

Dielectric-Loss-Limited Region. HSSP Seminar (2015): 3.26-3.27.
[ATTENUATION, DIELECTRIC LOSS, TRANSMISSION LINE] Slope of loss versus frequency. Implication for speed and distance scaling. (3 min.) Movie SD Movie HD

Differential (Microstrip) Trace Impedance. Newsletter v5-2 (1/22/2002).
[CHARACTERISTIC IMPEDANCE, DIFFERENTIAL SIGNALING] Many different combinations of height, width and spacing can generate the same differential impedance.

Differential Clocks. Newsletter v1-10 (9/4/1997).
[CLOCKS, DIFFERENTIAL SIGNALING] What's the impact of using differential clocks in a parallel bus?

Differential Coupling. EDN (11/13/2008).
[DIFFERENTIAL SIGNALING, TRANSMISSION LINE] Differential links need not be tightly coupled to work effectively.

Differential Crosstalk. Newsletter v3-20 (8/23/1999).
[CROSSTALK, DIFFERENTIAL SIGNALING] I have a number of high-speed differential PECL signals that I need to route in parallel on the PCB.

Differential Microstrip Geometry. HSSP Seminar (2015): 6.12.
[DIFFERENTIAL SIGNALING, LAYOUT, MICROSTRIP] Trade-offs Between Separation and Trace Width. (1 min.) Movie SD Movie HD

Differential Pair Skew. Newsletter v1-7 (8/5/1997).
[DIFFERENTIAL SIGNALING, SKEW] What impact does pair skew have on a received differential signal?

Differential Receivers Tolerate High-Frequency Losses. HSSP Seminar (2015): 6.22.
[ATTENUATION, DIFFERENTIAL SIGNALING] Effect of Receiver Thresholds on Signal Quality in the Face of Signal Dispersion. (3 min.) Movie SD Movie HD

Differential Receivers Tolerate High-Frequency Losses. EDN (11/28/2002).
[ATTENUATION, DIFFERENTIAL SIGNALING, DISPERSION, SERIAL LINK] Differential receivers have more accurate switching thresholds than ordinary single-ended logic.

Differential Reflections. Newsletter v2-21 (8/17/1998).
[DIFFERENTIAL SIGNALING, REFLECTIONS, TRANSMISSION LINE] Does the standard formula for reflections also apply to differential/balanced lines where two lines carry one signal?

Differential Routing. Newsletter v2-30 (11/11/1998).
[DIFFERENTIAL SIGNALING, LAYOUT] Is it better to route differential traces over/under (broadside) or side-by-side (edge-coupled)?

Differential Signaling (Through Connectors). Newsletter v3-12 (5/7/1999).
[DIFFERENTIAL SIGNALING] I have 16 differential line pairs that have to go through a connector. What signal to ground ratio and pattern should I use?

Differential S-Parameters. HSSP Seminar (2015): 6.62-6.64.
[DIFFERENTIAL SIGNALING, S-PARAMETERS] Practical advice.

Differential Stripline Geometry. HSSP Seminar (2015): 6.13-6.14.
[DIFFERENTIAL SIGNALING, LAYOUT, STRIPLINE] Also - Offset Stripline Geometry. (2 min.) Movie SD Movie HD

Differential TDR. EDN (8/22/2002).
[DIFFERENTIAL SIGNALING, PROBES, TESTING] A differential TDR instrument provides two outputs, x and -x, which you connect to the traces under test.

Differential Termination. HSSP Seminar (2015): 6.34-6.35.
[CIRCUIT TOPOLOGY, DIFFERENTIAL SIGNALING, TERMINATION] Common and Differential Modes of Termination. Achieving Both. (2 min.) Movie SD Movie HD

Differential Termination. EDN (6/8/2000).
[DIFFERENTIAL SIGNALING, TERMINATION] Terrible things can happen to the common-mode artifacts if your trace delay equals one-quarter of the clock period.

Differential Termination with Re-Biasing. HSDD Seminar (2015): 6.67.
[CIRCUIT TOPOLOGY, DIFFERENTIAL SIGNALING, TERMINATION] Clever ways to change the DC offset of your differential signal.

Differential-to-common-mode conversion. EDN (10/17/2002).
[DIFFERENTIAL SIGNALING, EMC] Any imbalanced circuit element within an otherwise well-balanced transmission channel creates a region of partial coupling between the differential and common modes of transmission at that point.

Differential Transitions. EDN (1/8/2009).
[CHARACTERISTIC IMPEDANCE, DIFFERENTIAL SIGNALING, REFLECTIONS] The trick of inserting nearby compensation to fix problems elsewhere within the transition region is the secret to successful transition design.

Differential U-Turn. EDN (9/1/2000).
[CONNECTORS, DIFFERENTIAL SIGNALING, SPLIT PLANES, STRIPLINE] What is the effect of a split in a solid plane on the impedance of a coplanar differential pair?

Diffrential Broadside-Coupled Geometry. HSSP Seminar (2015): 6.15-6.17.

[BROAD-SIDE COUPLING, DIFFERENTIAL SIGNALING] Asymmetry in Broadside Configuration. (6 min.) Movie SD Movie HD

Digital Receive-Based Equalization. HSSP Seminar (2015): 3.55-3.56.
[EQUALIZATION] Decision Feedback Equalizer. (2 min.) Movie SD Movie HD

Diode Termination. HSDD Seminar (2015): 6.63-6.64.
[CIRCUIT TOPOLOGY, EXAMPLES, TERMINATION] Limitations of the approach. Examples. (7 min.) Movie SD Movie HD

Diode Terminations. Newsletter v2-19 (7/28/1998).
[POWER DISSIPATION, TERMINATION, TRANSMISSION LINE] Is there any technical basis for concluding that diodes provide a "cleaner" signal?

Directionality of Crosstalk. ED (8/18/1997).
[CROSSTALK, LAYOUT] (Originally titled: The Real Truth About Crosstalk) If you are trying to manage crosstalk from first principles, so it comes out right on the first spin, look into the new crosstalk prediction tools that feature IBIS I/O modeling.

Distributed Nature of Inductance. HSNG Seminar (2015): 2.1-2.22.
[GROUND BOUNCE, INDUCTANCE] Difficulties with Observing Ground Noise. Implications for Measuring Voltages. Example Measurement: Inductance of Via. (20 min.) Movie SD Movie HD

Do Terminations Reduce Emissions?. HSNG Seminar (2015): 5.10-5.15.
[EMC, TERMINATION] Live Discussion of Signal Spectra. (2 min.) Movie SD Movie HD

Double-Tracking. Newsletter v7_05 (9/7/2004).
[BACK PLANE, CROSSTALK] Let’s begin this discussion looking at the belt-and-suspenders, super-safe differential stripline architecture.

Driving Heavy Loads. HSNG Seminar (2015): 2.78-2.82.
[CAPACITANCE, EE BASICS] VI Diagrams. Short-circuit current. Effect of oversize capacitive load. (8 min.) Movie SD Movie HD

Driving the World of Gigabit Ethernet. EDN (11/6/1997).
[GIGABIT ETHERNET] How should we best specify the I/O performance of drivers for the Gigabit Ethernet parallel interface?

Driving Two Loads. EDN (7/19/2001).
[LAYOUT, MULTI DROP, RINGING] Any time you build a split-tee, always simulate the circuit with a maximal degree of capacitive imbalance in the receivers.

Driving-Point Impedance. EDN (5/14/2009).
[REFLECTIONS, TERMINATION] In a perfect series-terminated architecture, you can measure the driving point impedance at the driver, in the middle of the line, or a hundred miles away, the measurement always returns the same number: Z0.

Dual Ground Shields. Newsletter v3-19 (8/12/1999).
[LAYER STACK, REFERENCE PLANES] Theoretically, if the planes are completely solid (no holes), they would act as near-perfect isolation boundaries, BUT you have to consider the holes…

Dual Transceivers. EDN (6/10/1999).
[LAYOUT, MULTI DROP, RISE TIME] You can make extremely small, zero-cost, high-performance switches from ordinary solder pads and solder paste.

Earth Ground. Newsletter v2-12 (5/7/1998).
[GROUNDING] The most important point to make with regard to grounding is that the input to every

digital logic gate is a DIFFERENTIAL amplifier.

ECL and PECL. Newsletter v2-22 (8/25/1998).
[LEVEL TRANSLATION] Can I directly connect a differential ECL signal to a differential PECL device?

ECL and PECL Reader Responses. Newsletter v2-23 (9/1/1998).
[LEVEL TRANSLATION] Further discussion of ECL-to-PECL level translation.

Effect of Capacitive Loads. HSDD Seminar (2015): 6.42-6.52.
[CAPACITANCE, CIRCUIT TOPOLOGY, REFLECTIONS] Single Load in Middle of Line. Multiple Loads. Slowing Down the Rise Time. Adjusting the End Termination. Key Equations. Idea for Design. (20 min.)
Movie SD Movie HD

Effects of Delay. HSDD Seminar (2015): 1.42-1.59.
[DELAY, LAYER STACK] Propagation Delay in Various Media. Example of Mixed Dielectric. Dielectric Properties of PCB Traces. Outer-Layer PCB Traces Are Faster. Distributed vs. Lumped Systems. Physical Length of Rising Edge. Pi Model of Transmission Line. Uses for The Pi Model. (52 min.)
Movie SD Movie HD

Effects of Source and Load Impedance. HSDD Seminar (2015): 4.11-4.17.
[TERMINATION, TRANSMISSION LINE] Exponential Decay. Time-Space Diagram. Ways to Achieve Signal Convergence. (22 min.) Movie SD Movie HD

EM Simulation Software. Bruce Archambeault. EDN (6/26/2008).
[EM FIELDS, EMC, SIMULATION] Dr. Bruce Archambeault, distinguished engineer at IBM, IEEE fellow, and the author of the "EMI/EMC Computational Modeling Handbook", responds to my questions about electromagnetic (EM) simulation software.

EMI Simulations Tools. EDN (3/2/1998).
[EMC, SIMULATION] (Originally titled: EMI Simulation Tools) Many EMI simulators are embellished with flashy demonstrations, which, like the smell of coffee brewing, or the sound of bacon frying, promise more than they can possibly deliver.

End Termination. HSDD Seminar (2015): 6.4-6.15.
[CIRCUIT TOPOLOGY, TERMINATION] Function of Split Termination. Design Constraints. Thevenin Equivalent Model of End Termination. Design Process. Design Solution. Reflections from a Capacitive Load. Effect of Stub Hanging Beyond End Termination. (36 min.) Movie SD
Movie HD

Endpoint Distortion. EDN (6/11/2009).
[REFLECTIONS, TERMINATION] The nature of instantaneous signal distortion at the receiver is defined by an equivalent circuit comprising two components: a series resistance and a shunt capacitance.

End-Termination of Differential Signals. HSDD Seminar (2015): 6.66.
[CIRCUIT TOPOLOGY, DIFFERENTIAL SIGNALING, TERMINATION] Differential and common-mode termination concepts. (8 min.) Movie SD Movie HD

Equalizers. HSSP Seminar (2015): 3.36-3.49.
[EQUALIZATION, EXAMPLES] PCB Trace Performance (graph). Received Signal at End of Line (waveform). Criteria for ISI Errors. ISI Criteria in the Frequency Domain. TTL/CMOS Levels Have Little ISI Tolerance. ISI Tolerance of Signaling Schemes. Time-Domain Response with 1st-Order Digital Equalizer. Digital Transmit Pre-emphasis Analysis. Effect of Equalization (1-m). Effect of Equalization (0.5-m). Digital EQ Eye Patterns for 10BASE-T Ethernet. Real backplanes. 4-Tap Transmit-Based Equalizer for PAM-4. (35 min.) Movie SD Movie HD

Equalizing Cables. EDN (8/2/2001).

[CABLES, EQUALIZATION] How do you equalize LVDS signals transmitted through cables of say 10 to 50m?

Equivalent Circuit Source Impedance. Newsletter v2-9 (3/23/1998).
[HIGH-SPEED DESIGN FORMULAS] What is the true source impedance of the equivalent circuit at figure 1.6 (page 13)?

Ernie's Story. ED (12/1/1996).
[ERNIE, MANAGEMENT] Engineers without a basic understanding of high-speed effects will likely end up just like Ernie, sitting in somebody else's office, fidgeting and sweating.

Erroneous Harmonics. Newsletter v4-9 (10/4/2001).
[BANDWIDTH] You won't find a quote in my book about "harmonics" because that isn't a good way to look at the problem.

ESR of Regulator Output Capacitor. Newsletter v5-3 (2/25/2002).
[BYPASS CAPACITORS, MANAGEMENT, POWER SYSTEMS] How can the ESR of a bulk capacitor (tantalum or electrolytic capacitor) affect a linear voltage regulator?

Essential System Margin. EDN (12/11/2003).
[ATTENUATION, MANAGEMENT, SERIAL LINK] You should make tiny artificially adjustments to every line in the budget until you drive the system margin to zero. Only you will know where these adjustments are hidden.

Example Geometries. HSDD Seminar (2015): 4.8-4.10.
[COAXIAL, LAYOUT, MICROSTRIP, STRIPLINE, TRANSMISSION LINE, TWISTED PAIR] Relations Between Impedance and Delay. (9 min.) Movie SD Movie HD

Example Jitter Measurements. HSNG Seminar (2015): 5.41-5.68.
[EXAMPLES, JITTER] Duty-cycle distortion. Effect of ringing. Effect of pair skew. Example of skew from DLL. Making a good low-jitter clock source. Jitter propagation.

Extra Fries, Please. EDN (1/7/1999).
[SKEW] In the high-speed world, timing is everything, so I predict that delay-compensated clock repeaters will be really hot.

Eye Don't Like It. EDN (11/9/2006).
[JITTER, SIMULATION, TESTING] An eye diagram makes a wonderful way to check finished system margins, but a terrible diagnostic tool.

Eye of the Probe. EDN (12/1/2006).
[PROBES, SIMULATION] If your probe loads the circuit and corrupts the physical measurement, how can you ever discern the "real signal" at C3 with no probe attached?

Factors That Reduce Ground Bounce. HSDD Seminar (2015): 2.8-2.17.
[DIFFERENTIAL SIGNALING, GROUND BOUNCE, POWER SYSTEMS, SPLIT PLANES] A Well-dispersed Array of Pwr/Gnd Pins. Differential Inputs. Shared Reference. Split-Power Architecture. (10 min.)
Movie SD Movie HD

Ferrite Beads. EDN (10/12/2000).
[FERRITE BEADS] Ferrite beads come in two flavors: high-Q, resonant beads and low-Q, non-resonant beads, also called lossy, or absorptive beads.

Fiber-Optic Encoding. EDN (1/10/2002).
[DATA CODING, GIGABIT ETHERNET] Codes that scramble the data post-coding cannot control either the DC balance or the maximum run-length of the scrambled output.

Field Cancellation. EDN (3/3/2011).
[EM FIELDS, MICROSTRIP] Eddy currents flowing in a solid reference plane underneath a pcb trace

partially cancel the magnetic fields emanating from that trace.

Finger the Culprit. EDN (6/21/2007).
[DELAY, TESTING] When debugging a rare mode of failure, never attempt a direct fix. The test cycles associated with each attempted improvement will kill your development schedule. Your first order of business is to make the problem worse.

Flex Cables. HSNG Seminar (2015): 4.73-4.78.
[EXAMPLES, LAYOUT, REFERENCE PLANES] Crosshatched Ground. Crosshatch Impedance. Crosshatch Crosstalk vs. Spacing (graph). (11 min.) Movie SD Movie HD

Flip-Flops. Newsletter v4-2 (5/12/2000).
[METASTABILITY] What actually causes the metastability in Flip- Flops?

(For Your) Protection. EDN (12/9/2004).
[ELECTROMIGRATION, ESD, OVERSHOOT, RINGING] Protection diodes have a limited lifetime—don't wear them out.

Four-Way Distribution. Newsletter v1-14 (10/17/1997).
[LAYOUT, MULTI DROP] How to best distribute a bus to four different loads.

Frequency Content of Digital Signals. HSDD Seminar (2015): 1.28-1.41.
[BANDWIDTH, EE BASICS, RINGING, RISE TIME] Data Band. Baud Interval Band (Rectangle = Step). Rising/Falling Edge Band. Frequencies That Matter for Digital Design. Meaning of "Frequency Response". Effect of Parasitics. Conceptual Frequency Response of Every PCB Trace. Relation of Knee Frequency to Circuit Performance. Effect of Shrinking Rise/Fall Time. International Technology Roadmap for Semiconductors (ITRS). (25 min.) Movie SD Movie HD

Frequency Offset, Wander, and Jitter. HSSP Seminar (2015): 12.46-12.59.
[CLOCKS, JITTER] Clock Recovery on a Serial Link. Clock Specifications. Why Are Oscillators Imperfect?. Effect of Frequency Offset in PLL Clock Recovery Circuit. Effect of Wander in PLL Clock Recovery Circuit. Racing Game Analogy for Understanding Tracking and Filtering Behavior. Your Tracking Filter. Decomposition of Trajectory. What's Better?. Car vs. PLL. Tracking Gain vs. Frequency. Effect of Resonance on Cascaded Systems. Effect of Large Multiplication Ratio. SONET Clock Architecture. (35 min.) Movie SD Movie HD

Frequency-Domain Analysis. HSSP Seminar (2015): 4.1-4.9.
[S-PARAMETERS] Why bother with the frequency domain?. Terminology of Frequency-Domain Analysis. Sine In, Sine Out. The advantage of LTI modeling. Information Necessary to Characterize an LTI System. Is a Digital Driver LTI?. Frequency-Based Analysis. (13 min.) Movie SD Movie HD

Frequent Obsession. EDN (10/12/2006).
[BACK PLANE, BANDWIDTH, TESTING] Frequency-domain instruments can play an important role in the measurement process, but should not be the main focus of your specification.

Front-Connected Power Supply. Newsletter v4-17 (12/5/2001).
[EMC, GROUNDING, POWER SYSTEMS] Why connections on the front side of a plug-in card are a bad idea.

Fundametals of PCB Design. Web (8/16/2010).
[LAYOUT, POWER DISSIPATION] This introductory overview of printed-circuit design treats the main difficulties you will likely meet when planning, designing, and manufacturing printed circuit boards for digital applications.

(The) Future of On-Chip Interconnections. EDN (2/3/2000).
[INTERCONNECTIONS, MULTI LEVEL] Today's chip-layout software takes into account the RC

propagation delays of major bus structures and clock lines. In tomorrow's designs, at even higher speeds, the full RLC nature of the on-chip transmission channels will emerge.

Gigabit Ethernet. PCD (2/1/1997).
[GIGABIT ETHERNET] Gigabit Ethernet is going to be faster, with more parallel signals, and tighter layout constraints.

Gigabit Ethernet Examples. HSDD Seminar (2015): 6.74-6.82.
[DIELECTRIC LOSS, DISPERSION, EXAMPLES, REFLECTIONS, SKIN EFFECT, TRANSMISSION LINE] Serial interface at 1.25 Gb/s. Showing dielectric loss and skin effect. Showing effect of vias and mismatched terminations. Showing effect of both-ends termination vs. single-end.

Gigabit Ethernet Specification. Newsletter v2-6 (2/2/1998).
[GIGABIT ETHERNET] The GMII is designed as a chip-to-chip interface. The expected link distance is therefore about 3 to 12 inches.

Going Non-linear. EDN (5/16/2002).
[SIMULATION] Spice is grand for non-linear circuits, but if your circuit is linear you might question whether it is best. The FFT shines as an efficient computational tool for long transmission channels.

Going Vertical. EDN (10/14/1999).
[EMC] Keeping your traces close to a solid, uninterrupted reference plane is one of simplest, most effective things you can do to reduce electromagnetic radiation and harden your product against ESD.

Ground Bounce Calculations. Newsletter v1-12 (9/26/1997).
[HIGH-SPEED DESIGN FORMULAS] On page 62 of the High-Speed Digital Design Text… where does the factor of 1.52 come from?

Ground Current. Newsletter v3-7 (3/15/1999).
[LAYER STACK, RETURNING SIGNAL CURRENT] Details the exact path of returning signal current when a chip switches HI or LO

Ground Fill. EDN (5/26/2005).
[EMC, GROUNDING, REFERENCE PLANES] Isolated, discontinuous regions of ground fill do not help reduce magnetic-field coupling between traces or radiation from the board.

Ground Fills. Newsletter v1-3 (6/24/1997).
[EMC, GROUNDING, REFERENCE PLANES] The "poured ground" (more commonly called a "ground fill") is a technique useful on two-layer boards for reducing crosstalk due to ELECTRIC FIELD coupling. Superceded by "Ground Fill", EDN 26 May 2005.

Ground Loops. EDN (12/18/2012).
[CROSSTALK, GROUNDING] Single-point ground networks provide isolation only when communications remain localized to isolated sections of the network.

Ground Plane Slots. HSDD Seminar (2015): 5.24-5.32.
[CROSSTALK, REFERENCE PLANES, RETURNING SIGNAL CURRENT, TRANSMISSION LINE] Traces Passing Over a Ground Plane Slot. Crosstalk From Ground Plane Slots. Connector Layout Slots. Crosstalk Versus Trace Separation Experiment. Crosstalk Over a Slotted Ground Plane (waveforms). Crosstalk Over a Slotted Ground Plane (graph). Why Wasn't the Lower Plane Very Effective? (20 min.) Movie SD Movie HD

Ground/Power Planes. Newsletter v1-8 (8/15/1997).
[GROUNDING, LAYER STACK, POWER SYSTEMS] At very high speeds, bypass capacitance needs to be within less than 1/10 of a rising-edge-length in order to function effectively.

Guard Traces. Newsletter v15_02 (5/17/2012).

[CROSSTALK] A guard trace, or guard track, is a pcb trace that is installed parallel to an existing high-speed signal. Guard traces are usually installed in the hope of reducing crosstalk.

Hairball Nets. Newsletter v4-10 (10/8/2001).
[LAYOUT, MULTI DROP, TERMINATION] Terminating big globs of unstructured loads.

Hairball Networks. HSSP Seminar (2015): 12.20-12.34.
[MULTI DROP] To Tee or Not To Tee. Basic Tee with No Termination. Add Receivers (and ESD Diodes). Tee with Slow Driver. Tee with Both-Ends Termination. Tee with Weak End Termination. Tee with Sneaky Impedance Adjustment. Tee with Series Termination. Unbalanced Tee with Series Termination. Unbalanced Tee with End Termination. Unbalanced Tee with Distributed Damping. Apply Your Knowledge: Check the "H" For Resonance.. (27 min.) Movie SD Movie HD

Half Measures. EDN (1/5/2006).
[POWER DISSIPATION, REFLECTIONS, TERMINATION] (Regarding series termination) a good energy-balance equation often easily sums up the operation of a complicated system without bogging you down in details.

Healthy Power. EDN (3/30/2000).
[ERNIE, POWER SYSTEMS] When your prototype board comes back from fabrication, take the time to check the health of its power system.

Hidden Schematic. Bruce Archambeault. EDN (5/25/2006).
[EMC, GROUNDING] Dr. Bruce Archambeault, creator of the IBM EMC rule-checking program "EMSAT", says "Ground is a good place to grow potatoes and carrots", but a poor concept for high-frequency engineering.

High-Speed Backplane Connectors. EMC Soc (8/17/2011).
[BACK PLANE, CONNECTORS, CROSSTALK] Discusses the main factors affecting backplane connector performance, and predicts the future of backplane connector development.

High-Speed Digital Design Book. About the Book (11/8/2015): 0.0-0.0.
[EE BASICS, MANAGEMENT] Considered the original "bible" of high-speed design issues, High-Speed Digital Design focuses on a combination of digital and analog circuit theory. This comprehensive volume helps engineers who work with digital systems shorten their product development cycles and fix their latest high-speed design problems.

High-Speed Digital Design Seminar. About the Seminar (11/8/2015): 0.0-0.0.
[EE BASICS, MANAGEMENT] A practical two-day seminar course about building high-speed digital hardware. It is filled with examples, explanations, and classroom demonstrations. Anyone who works with high-speed digital signals will understand and benefit from the material presented.

High-Speed Digital Design: Opening Lecture. HSDD Seminar (2015): 1.1-1.5.
[EE BASICS, MANAGEMENT] Definition of Signal Integrity. Relation to EMI. Purpose of Studying Signal Integrity. Overview of Program. (9 min.) Movie SD Movie HD

High-Speed Digital Design: Overview Article. MTT-9 (8/15/2011).
[EE BASICS, MANAGEMENT] This survey article highlights key similarities, and important differences, between high-speed digital and microwave hardware, addressing factors related to transmitters, transmission pathways, receivers, and the people who design them.

High-Speed Noise and Grounding Seminar. About the Seminar (11/8/2015): 0.0-0.0.
[EE BASICS, MANAGEMENT] This course focuses on mixed-signal applications involving high-speed digital electronics used in conjunction with sensitive analog circuits such as radio receivers, GPS devices and cell phones. This course addresses the critical issues of noise and grounding that are seen in many advanced signal processing applications today, including avionics, telemetry and guidance systems.

High-Speed Noise and Grounding: Opening Lecture. HSNG Seminar (2015): 1.1-1.5.

[EE BASICS, MANAGEMENT] Definition of Noise and Grounding Subject Matter. Purpose of Studying Noise and Grounding. Overview of program. (4 min.) Movie SD Movie HD

High-Speed Return Signals. Newsletter v1-15 (10/27/1997).
[LAYER STACK, RETURNING SIGNAL CURRENT] How do high speed return signals travel on a 4 layer pc board?

High-Speed Signal Propagation Book. About the Book (11/8/2015): 0.0-0.0.
[EE BASICS, MANAGEMENT] This is an advanced-level reference text for experienced digital designers who want to press their designs to the upper limits of speed and distance.

High-Speed Signal Propagation Seminar. About the Seminar (11/8/2015): 0.0-0.0.
[EE BASICS, MANAGEMENT] This is an advanced-level course for experienced digital designers who want to press their designs to the upper limits of speed and distance. Focusing on lossy transmission environments like backplanes, cables and long on-chip interconnections, this two-day course teaches a unified theory of transmission impairments that apply to any transmission media.

(Advanced) High-Speed Signal Propagation: Opening Lecture. HSSP Seminar (2015): 1.1-1.4.
[EE BASICS, MANAGEMENT, SERIAL LINK] Delineation of Material to be Covered. Prerequisites. Overview of Program. (5 min.) Movie SD Movie HD

Holding On. EDN (7/9/2009).
[REFLECTIONS, TERMINATION] The tri-state feature, if available in your driver, acts as a sort of additional short-time dynamic memory element that you can use to extend the hold time of your driver.

Hot Plugging and Beefy Guys Named Mark. EDN (11/5/1998).
[HOT PLUGGING, POWER SYSTEMS] Mark McGwire reminds me of some of the technicians I have seen working on large systems

How Close is Close Enough?. EDN (4/9/1998).
[LAYOUT, TERMINATION] How close to the driver must you keep your series terminations?

How Fast is Fast?. EDN (7/2/1998).
[RINGING] In digital systems, the frequencies of interest depend on the edge transition time of the logic involved.

How Many Segments. Newsletter v12_07 (12/9/2009).
[RISE TIME, SAMPLED DATA, SIMULATION] Examples show effect of inadequate number of segments in piece-wise linear (PWL) approximation.

How Solid Plane Layers Control Crosstalk. HSDD Seminar (2015): 5.1-5.10.
[CROSSTALK, REFERENCE PLANES, TRANSMISSION LINE] Early Computers vs. Multilayer PCB. Microstrip Response to Changing Magnetic Field. Magnetic Field Animations. Do Not Give Your PCB Vendor Full Control Over H and W. How Much Crosstalk Can You Take?. Where Simulation Fails Us. (21 min.)
Movie SD Movie HD

I Still Love the BGA. Newsletter v2-10 (4/6/1998).
[CHIP PACKAGING] Hate mail, mostly from mechanical designers and production test engineers, about BGA's

IBIS. PCD (4/1/1997).
[SIMULATION] IBIS is going to solve a lot of common, everyday, high-speed design problems, but, first we have to get our chip vendors to provide IBIS model files for every part they make.

IBIS I/O Buffer Information Specification. HSDD Seminar (2015): 2.22-2.28.
[SIMULATION] Live discussion of the purpose and appropriate use of modeling software. (6 min.)
Movie SD Movie HD

IBIS Simulation with Gaussian Edges. HSDD Seminar: 2.29-2.33.
[RISE TIME, SIMULATION] Simulation artifacts caused by the use of piecewise-linear (PWL) Spice sources. Presentation of Gaussian source useful for eliminating the artifacts.

Imperfections in Shield Coverage. HSNG Seminar (2015): 4.59-4.62.
[COAXIAL, GROUNDING, SHIELDING] Shielding Effectiveness (Shield-Current Transfer Impedance). Direct Attachment of Coax to Chassis. Coaxial Shield Circuit Theory. (17 min.) Movie SD Movie HD

Impulsive Behavior. EDN (12/2/2010).
[EE BASICS, SAMPLED DATA] Stimulate any linear system with one short, intense pulse, and you see a response characteristic of that particular system.

In-Between Spaces. EDN (5/24/2007).
[EM FIELDS, VIAS] According to Kirchoff's laws for circuit analysis, the total inductance of two inductors placed in series should equal the sum of their independent inductances; this is not true for parasitic inductances in high-speed digital circuits.

Inducing Metastability. Newsletter v4-4 (6/4/2001).
[METASTABILITY, SKEW] What if I *WANT* to induce the metastable state in a flip-flop?

Inductance. HSNG Seminar (2015): 1.31-1.52.
[EXAMPLES, INDUCTANCE] Current Does Not Flow Instantaneously. Every Loop Has Inductance. Simple Inductance Test Circuit. Inductance of Circular Loop (Empirical). Inductance of Hairpin and Other Structures. Inductance of Wire Above Solid Plane. Why All the Fuss About Inductance?. Mutual Inductance Matters. What About Electromagnetic Radiation? (27 min.) Movie SD Movie HD

Inductance of Bypass Capacitor. HSDD Seminar (2015): 8.1-8.13.
[BYPASS CAPACITORS, INDUCTANCE, LAYOUT, SILAB HSDD] Electrical performance model useful for capacitor types. (41 min.) Movie SD Movie HD

Inductance of PCB Via. HSSP Seminar (2015): 5.44-5.51.
[EXAMPLES, INDUCTANCE, SILAB HSSP, VIAS] Conditions of Measurement. Path of Return Current. Measuring Incremental Parameters. Four-Terminal Inductance Measurement. Step-Response Measurement of Inductance. Measured Data. Impedance of a Via. (32 min.) Movie SD Movie HD

Initial Condition. EDN (1/10/2008).
[TERMINATION, TRANSMISSION LINE] A split termination biases the line at a halfway voltage so that the driver need only source or sink enough current to swing the line halfway in either direction.

Intentional Clock Modulation. EDN (8/3/1998).
[CLOCKS, EMC, JITTER] Over the years, various techniques have been proposed for modulating, or dithering, the clock frequency to break up the accumulated spectral power into a larger number of new modes.

Intentional Overshoot. EDN (8/7/2003).
[CLOCKS, OVERSHOOT, SKEW] Ernie reduces the value of his series terminator, inducing some intentional overshoot that partially compensates for the lack of vivre in the received signal and speeding up (slightly) the threshold crossing.

Interconnections Between Boxes. HSNG Seminar (2015): 4.47-4.57.
[CROSSTALK, EXAMPLES, MIXED SIGNALS, SILAB HSNG] Adapted from Mixed-Signal Isolation, Part II: "RF Crosstalk" (live discussion) Coaxial Cables and Connectors. Test Arrangement for measuring crosstalk (slide 60). Extending the Dynamic Range of Your Scope. Increase Level of Aggressor. Example Measurement: Coaxial Shield Effectiveness. (17 min.) Movie SD Movie HD

Interconnections Matter. EDN (5/13/1999).
[INTERCONNECTIONS] When you look at a digital machine, if you are not looking at the interconnections, you are missing one of the most important parts of the structure.

Interplane Capacitance. Newsletter v3-21 (8/30/1999).
[LAYER STACK, POWER SYSTEMS, RETURNING SIGNAL CURRENT] Follow-up to "High-Speed Return Signals" newsletter v1-15, discusses the effective useful radius of the interplane capacitance.

It's a Gaussian World. EDN (1/7/2010).
[BANDWIDTH, RISE TIME] My previous article, "Real Signals" (EDN Oct. 08, 2009), suggests that most digital output waveforms follow a nearly Gaussian profile. Let's test that theory with a real-world measurement.

Jitter and Phase Noise. Newsletter v4-7 (6/25/2001).
[CLOCKS, JITTER] Converting spectral-power-density noise measurements into rms and peak-to-peak jitter.

Jitter and SNR Combined. Newsletter v7_06 (11/18/2004).
[CLOCKS, JITTER] I would rather not consider of the joint probability of occurrence of vertical noise and horizontal jitter in the same equation.

Jitter Capture. Newsletter v13_01 (3/19/2010).
[JITTER, TESTING] If you want to measure jitter the same way your receiver sees it, program your jitter measurement equipment to mimic your receiver's PLL tracking algorithm.

Jitter Characterization. Newsletter v11_06 (10/8/2008).
[JITTER, TESTING] I wish I could begin by stating the definition of jitter. Wouldn't it be great if there was only one definition? Unfortunately, the subject isn't that simple. Here's a sampling of definitions from various sources.

Jitter Creation. Newsletter v12_06 (10/8/2009).
[JITTER, TESTING] Here is a simple and effective jitter-creation circuit you can use in your own laboratory to create calibrated amounts of jitter. Observing this source, you can try all the features of your jitter-measurement equipment to see what they all do.

Jitter Measurement. Newsletter v3-22 (10/21/1999).
[JITTER, TESTING] What is the best way to measure Signal jitter using a Digital Oscilloscope?

Jitter Reference Clock Settings. Newsletter v15_03 (8/21/2012).
[JITTER, TESTING] You can never measure (or even define) the meaning of jitter in any absolute sense. All you can do is compare one signal against another and measure the difference in zero-crossing times between the two waveforms.

Jitter Specifications. HSSP Seminar (2015): 12.60-12.74.
[JITTER, TESTING] Appearance of Jitter. Jitter Histogram. Decomposition of Jitter Histogram. Extrapolation of Random Jitter. Deterministic vs. Random Jitter. Extra for Experts: Jitter Measurement Techniques. Measuring Deterministic Jitter. Measuring Random Jitter. Combining Deterministic and Random Jitter. Fudge Factors for Random Gaussian Jitter. Time-Interval Analysis (TIA). Golden-PLL Method for Measuring Jitter. BERT Scan. Spectral Measurement of Jitter Variance. (19 min.) Movie SD Movie HD

Jitter Tracking. Newsletter v13_02 (9/3/2010).
[JITTER, TESTING] A deep grasp of jitter, wander, and how a PLL reacts to them will help refine your understanding of serial data communications.

Jitter-Free Clocks. EDN (8/5/1999).
[CLOCKS, EMC, JITTER] Is there any way to make a timing reference that has low jitter and low spectral peaks and at the same time is compatible with zero-delay-repeater structures?

(The) Jitters. ED (1/20/1997).
[CLOCKS, JITTER] If you are using a clock multiplier, or a PLL-based clock regenerator, make sure to comply with the specifications for offset, wander, and jitter on the reference clock input.

Keeping Up With Moore. EDN (5/7/1998).
[MANAGEMENT] multi-layer pc-boards, solid power and ground planes, surface-mount technology, reflow soldering, and the BGA package were the prominent advances in packaging during the last 20 years.

Killer Packet. Newsletter v5-7 (6/7/2002).
[DATA CODING] Scrambling by itself does *nothing* to improve the worst case DC balance.

Law of Product Development. Newsletter v8_06 (10/3/2005).
[ATTENUATION, TERMINATION] Regarding attenuating terminations, "The more independant requirements you place on a circuit, the more complex the circuit must become."

Layer Transitions. HSDD Seminar (2015): 5.47-5.49.
[LAYER STACK, LAYOUT, REFERENCE PLANES] Implications for Fast Signals. Best Way to Route the Board. (5 min.) Movie SD Movie HD

Lightning Example. HSNG Seminar (2015): 4.79-4.83.
[EM FIELDS, EXAMPLES] Lightning EMF Equivalent Circuit. Lightning Balls. (4 min.) Movie SD Movie HD

Line Length. Newsletter v3-14 (6/7/1999).
[REFLECTIONS, RINGING] The critical line length beyond which many people use terminators varies from about 1/10 to 1/3 the length of the rising edge.

Linear System Theory (Supplemental). HSSP Seminar (2015): 4.21-4.28.
[S-PARAMETERS] Theory of Linearity. Theory of Linear Superposition. Theory of Time-Invariance. Convolution. Comparison of Time- and Frequency-Domain Approaches.

Linearity. EDN (9/9/2010).
[EE BASICS] Linearity is one of two properties essential for good signal fidelity, audio or otherwise. The other property is time-invariance.

Locating Reflections. HSSP Seminar (2015): 6.41-6.48.
[PROBES, TESTING] Probe technique.

Logic Analyzer Test Points. Newsletter v3-2 (1/21/1999).
[PROBES] The input impedance of the logic analyzer probe… makes a good deal of difference

Lossless Propagation. EDN (12/3/2007).
[ATTENUATION, CHARACTERISTIC IMPEDANCE, DISPERSION, TRANSMISSION LINE] In the short term, the input impedance of a uniform, lossless, distortionless transmission line appears purely resistive.

Lumped-Element Behavior. HSSP Seminar (2015): 3.8-3.14.
[CAPACITANCE, INDUCTANCE, REFLECTIONS] Lumped-Element Modeling. Limits to Lumped-Element Analysis. Pi-Model for LC mode. Pi-Model Special Cases. Reflection Coefficients for Reactive Loads. Reflection From Capacitive Load (Derivation). (10 min.) Movie SD Movie HD

Lumped-Element Crosstalk. HSDD Seminar (2015): 1.60-1.81.
[CAPACITANCE, CROSSTALK, INDUCTANCE] Step Response Theory. How Resistive Loading Changes Circuit Delay. Mutual Capacitance and Mutual Inductance. Measurement of Mutual Coupling. Comparison of Inductive and Capacitive Crosstalk. A Faraday Cage Fixes Capacitive Coupling. Mutual Inductance is a Current-Flow Problem. Improving the Return Path Fixes Inductive Crosstalk. Why Many Engineers Think First About Capacitance. (38 min.) Movie SD Movie HD

Main Points Not Taught in College. HSNG Seminar (2015): 1.53-1.56.
[BACK PLANE, DIFFERENTIAL SIGNALING] Logic Gates Are Differential Amplifiers. Digital Signals Have a Limited Bandwidth. Frequencies That Matter for Digital Signals. (9 min.) Movie SD Movie HD

Make It Better. EDN (2/26/2013).
[CHARACTERISTIC IMPEDANCE, RINGING] When the driver output resistance in the falling direction must be less than the output resistance in the rising direction, a common situation in CMOS totem-pole drivers, no value of series-terminating impedance can possibly make both edges perfect.

Making Gaussian Edges. EDN (12/3/2009).
[RISE TIME] This analog filter network converts each input step into a smooth, Gaussian-shaped rising and falling edge.

Making Noise. EDN (9/15/2005).
[POWER SYSTEMS, TESTING] A massive array of sources creates a huge amount of noise useful for testing power supply noise immunity.

Manager's Guide to Digital Design. EDN (4/8/2010).
[MANAGEMENT] This one-page executive summary includes everything a manageer needs to know about high-speed digital design. (April 8, 2010).

Managing Scotty. EDN (6/7/2001).
[MANAGEMENT] Scotty to Kirk, "We cannot get the shields back in less than an hour, Captain. The Klingon attack cracked our DiLithium crystal, and there's antimatter leaking everywhere..."

Managing Trace Skew. HSSP Seminar (2015): 6.39-6.40.
[SKEW] Analysis of Skew Magnitude. Effect of Circuit Floorplanning. (5 min.) Movie SD Movie HD

Margin Testing. JP Miller. EDN (3/3/2005).
[CROSSTALK, MANAGEMENT, TESTING] Testing a link in isolation is never sufficient; links must be tested in combination with other noise sources.

Matching Pads. EDN (12/21/2000).
[CABLES, LAYOUT, REFLECTIONS, TERMINATION] The only passive circuits that guarantee good impedance translation for wideband signals are resistive pads.

Matching to an External Cable. HSSP Seminar (2015): 6.23.
[DIFFERENTIAL SIGNALING, EMC, EXAMPLES] Example of Well-Balanced Interface. (3 min.) Movie SD Movie HD

Measured Data. HSDD Seminar (2015): 8.14-8.19.
[BYPASS CAPACITORS, EXAMPLES, INDUCTANCE, LAYOUT] Surface-Mounted Configurations. Inductance of Surface-Mounted Layouts (table). New Surface-Mounted Packages. AVX Interdigitated Capacitor (IDC). (6 min.) Movie SD Movie HD

Measuring Characteristic Impedance. HSSP Seminar (2015): 3.28-3.31.
[CHARACTERISTIC IMPEDANCE, TESTING, TRANSMISSION LINE] Influence of Losses on TDR Measurement. (9 min.) Movie SD Movie HD

Measuring Connectors. EDN (5/10/2001).
[CONNECTORS, CROSSTALK, TESTING] I would like to replace one connector type with a different, less expensive model. How do I prove the two connectors have the same electrical characteristics?

Measuring Droop. EDN (2/3/2005).

[POWER SYSTEMS, PROBES] What is the best technique to make DC voltage measurement on a power rail? Will a four-point measurement technique be the most accurate?

Measuring Nothing. EDN (4/23/2013).
[EM FIELDS, GROUNDING, PROBES, TESTING] When looking at a noisy, jittery signal, how can you tell which parts of the signal are "real" and which parts derive from noise and interference?

Measuring Power and Ground. Newsletter v3-13 (5/21/1999).
[POWER SYSTEMS] Follow-up to "Measuring Power-to-Ground Impedance", nwsltr v2-14

Measuring Power-Plane Resonance. Newsletter v2-27 (10/15/1998).
[POWER SYSTEMS] James Mears of National Semiconductor describes his experience attempting to measure the impedance between power-and-ground planes.

Measuring Power-Ground Impedance. Newsletter v2-14 (5/26/1998).
[POWER SYSTEMS] How to convert network-analyzer measurements of the impedance between a pair of power-and-ground planes from dB to ohms. Suggestions on probe configuration.

Measuring Shadows. EDN (3/26/2013).
[PROBES, TESTING] Measurements never reveal the thing you wish to know, only the shadow of that thing.

Measuring Skew. EDN (2/5/2004).
[PROBES, SKEW] You can't depend on automatic de-skewing when measuring tightly coupled differential systems.

Memory Bus Crosstalk. Newsletter v9_06 (8/22/2006).
[CHARACTERISTIC IMPEDANCE, CROSSTALK, JITTER] I am currently working on high speed memory bus with "interconnect jitter". My memory team recommends changing the bus geometry to improve timing.

Metastability in Flip Flops. Newsletter v3-15 (7/14/1999).
[METASTABILITY] What happens if you have two flip-flops in series, both using the same clock, and the first one goes metastable?

Metastability of a Flip-Flop. HSDD Seminar (2015).
[METASTABILITY, RELIABILITY, SILAB HSDD] Principle of metastability. When it matters. How to mitigate it. (29 min.) Movie SD Movie HD

Metastable Persons. EDN (3/16/2000).
[METASTABILITY] When you violate the setup-and-hold times on a flip-flop, the output might erratically go high, stay low, or pop one way and then back again.

Millions and Billions. EDN (8/18/2005).
[BACK PLANE, RISE TIME, SERIAL LINK] When considering any aspect of your circuit geometry, the relation between physical size and risetime helps determine the relative importance of that object in the overall scheme of the circuit.

Minimum-Inductance Distribution of Current. Newsletter v6_07 (7/22/2003).
[EM FIELDS, RETURNING SIGNAL CURRENT] Faraday, in his mind's eye, saw lines of force traversing all space.

Mitigating Crosstalk. Newsletter v6-01 (1/20/2003).
[CROSSTALK, DIFFERENTIAL SIGNALING, LAYOUT] What can be done to reduce the amount of crosstalk in a pcb.

Mixed-Signal Isolation: Part I. HSNG Seminar (2008).
[CROSSTALK, GROUNDING, MIXED SIGNALS, SILAB HSNG] (2008 release) Audio Frequency Interference. This movie is played in HSNG Chapter 4. (34 min.) Movie SD Movie HD

Mixed-Signal Isolation: Part II. HSNG Seminar (2008).
[CROSSTALK, GROUNDING, MIXED SIGNALS, SILAB HSNG] (2008 release) RF Crosstalk, RF Cables, and RF Connectors. Parts of this movie are performed live in HSNG Chapters 4 and 6. (33 min.)
Movie SD Movie HD

Mixed-Signal Isolation: Part III. HSNG Seminar (2008).
[CROSSTALK, GROUNDING, MIXED SIGNALS, SILAB HSNG] (2008 release) Achieving 120dB Isolation, PCB Traces at RF. This movie is played in HSNG Chapter 6. (29 min.) Movie SD Movie HD

Mixtures of skin-effect and dielectric loss. EDN (9/19/2002).
[DIELECTRIC LOSS, DISPERSION, SKIN EFFECT] Long, high-speed pcb traces operate in a zone influenced by both skin-effect and dielectric losses. Both mechanisms attenuate the high-frequency portion of your signals, but in slightly different ways.

Moat and Drawbridge Construction. HSNG Seminar (2015): 3.52-3.55.
[CROSSTALK, MIXED SIGNALS, RETURNING SIGNAL CURRENT, SPLIT PLANES] Efficacy of Ground Cuts at RF. The Cut Does NOT Eliminate RF Crosstalk. (14 min.) Movie SD Movie HD

Moats and Floats. ED (2/17/1997).
[EMC, GROUNDING, SPLIT PLANES] How to conduct multiple comparative layout studies in one pcb fabrication cycle.

Modeling Skin Effect. EDN (4/12/2001).
[BANDWIDTH, DELAY, RISE TIME, SIMULATION, SKIN EFFECT] Why does high-frequency current flow only on the outer surface of a printed-circuit trace?

Multilayer Routing. HSDD Seminar (2015): 5.33-5.42.
[CROSSTALK, GUARD TRACE, LAYOUT] Power and Ground Fingers. Cross-Hatched Ground Grid. Guard Trace on a Two-Layer Board. Guard Trace on Multilayer Board (classroom demo covers slides 5.37 - 5.42). (15 min.) Movie SD Movie HD

Multi-Level Signaling -- Designcon2000. DesignCon 2000 (1/30/2000).
[BACK PLANE, MULTI LEVEL, SERIAL LINK] multi-amplitude signaling won't help much below 2.5 Gb/s, however, at higher speeds where the loss slope increases MAS becomes very useful.

Multiple ADC grounding. EDN (2/1/2001).
[GROUNDING] Several of you wrote about "ADC Grounding" (EDN, Dec 7, 2000, pg 36) to ask what happens when you have more than one ADC.

Multiple Loads at End of Series-Terminated Line. HSDD Seminar (2015): 6.59.
[CAPACITANCE, TERMINATION, TRANSMISSION LINE] Effect on signal risetime.

Musical Interference. EMC Soc Nwsltr (7/1/2002).
[EMC] When you can walk up to your equipment and make it play Dixie on an AM radio, you will have captured the attention of your digital engineers.

Mutual Understanding. EDN (1/1/1998).
[CONNECTORS, CROSSTALK] A connector configured with too few power and ground pins, or with too many heavy loads, generates a lot of crosstalk.

Mysterious Ground. EDN (2/7/2002).
[GROUNDING, PROBES] All good probes come with short, tiny ground attachments. For single-ended measurements, don't depend on mysterious ground connections. Always use a good, short ground connection.

NASA Layer Stack. HSDD Seminar (2015): 5.50-5.52.
[LAYER STACK, LAYOUT, REFERENCE PLANES] Extemporaneous discussion of NASA layer stack. (3 min.)

Movie SD Movie HD

Nasty ESD Testing. Newsletter v4-13 (10/24/2001).
[ESD, TESTING] A thin, plastic package sitting on a metal desk, with wires hanging out the back of the package will prove embarrassingly susceptible to ESD.

Nature of ESD. EDN (8/6/2009).
[ESD] Once inside your product, ESD transient currents spread far and wide regardless of any ground jumpers, 100K resistors, and transorbs that may exist.

Negative Delay. EDN (8/30/2001).
[CLOCKS, DELAY, SKEW] If Congress invented negative-delay legislation, it might improve its reputation for alacrity.

Nibble Effect. Newsletter v12_03 (3/26/2009).
[BACK PLANE, TRANSMISSION LINE] A distributed bus simultaneously activates more than one driver. The timing on a distributed bus is as intricately planned as a ballet.

Nickel Matters. EDN (10/23/2012).
[SKIN EFFECT, TESTING] Nickel plating substantially increases the high-frequency resistance of a pcb trace. It lengthens the step response of the trace, exacerbating both inter-symbol interference and jitter.

Nickel-Plated Traces. Newsletter v5-6 (4/22/2002).
[ATTENUATION, SKIN EFFECT] We have been advised that due to the changes to the skin effect caused by the Ni/Au on the traces for high frequency RF designs we could be building in a problem.

Noise Isolation. Newsletter v2-13 (5/19/1998).
[CROSSTALK, GROUNDING, REFERENCE PLANES] Achieving isolation greater than 80 dB.

Noise Partitioning. W. Michael King. EDN (3/4/2004).
[CROSSTALK, EMC] Keep your loud, high-powered partitions from interfering with your little-bitty quiet ones.

Non-TEM Mode Example. HSSP Seminar (2015): 3.34-3.35.
[DISPERSION, EXAMPLES, NON-TEM, TRANSMISSION LINE] Comparing skin-effect, dielectic, and non-TEM dispersion effects.

Not all EMC engineers are bald. EDN (1/24/2002).
[EMC, MANAGEMENT] If you want to keep doing what you love to do you must constantly re-educate yourself.

Not Your Fault. EDN (3/5/2009).
[GROUNDING, POWER SYSTEMS] Green safety wires do not form a reliable single-point ground reference.

OFC Madness. EDN (3/1/2007).
[POWER SYSTEMS] Ernie heard that ofc cryogenic power cables are really good, but very expensive ($100's). Should he buy one?

On-Chip Bypassing with End Terminations. EDN (5/27/2004).
[BYPASS CAPACITORS, CHIP PACKAGING, POWER SYSTEMS, TERMINATION] On-chip capacitors have no effect on single-ended systems with symmetrically-split end-terminations.

On-Chip Bypassing with Series Terminations. EDN (4/29/2004).
[BYPASS CAPACITORS, CHIP PACKAGING, POWER SYSTEMS, TERMINATION] On-chip capacitors perform brilliantly in a series-terminated architecture.

One Measurement. Lockheed Luncheon (3/15/2013): 0.0-0.0.
[MANAGEMENT, PROBES, TESTING] Measurements define the body of knowledge we call Signal

Integrity. Master the technique of making proper measurements and you will become a guru of the art.

Onset of Non-TEM Behavior. HSSP Seminar (2015): 3.32-3.33.

[DISPERSION, EXAMPLES, NON-TEM, TRANSMISSION LINE] Equations for Estimating. (5 min.) Movie SD Movie HD

Open-Drain Lines. Newsletter v2-5 (2/9/1998).
[OPEN DRAIN, TERMINATION] Should I use one pull-up resistor located somewhere in the middle of my line, or two resistors of twice the value located at each end?

Operating Above Resonance. ED (4/14/1997).
[BYPASS CAPACITORS, LAYOUT] It's OK to use a bypass capacitor well above its point of series-resonance. That's the normal mode of operation for most bypass capacitors.

Overview of Termination Types. HSDD Seminar (2015): 6.1-6.3.
[RINGING, TERMINATION, TRANSMISSION LINE] Systems that suffer ringing benefit from termination. Over-damped circuits do not. (8 min.)

Parallel Resonance. EDN (2/2/2012).
[EE BASICS, POWER SYSTEMS] You can determine the peak of a parallel-resonant circuit step response from a graph of its inductive and capacitive asymptotes.

Parasitic Inductance of Bypass II. Newsletter v6_09 (12/1/2003).
[BYPASS CAPACITORS] The following values for the inductance of a surface-mounted bypass capacitor were collected using the step-response technique described in chapter 8 of High-Speed Digital Design.

Parasitic Inductance of Bypass Capacitors. EDN (7/20/2000).
[BYPASS CAPACITORS, LAYOUT] You can estimate the parasitic series inductance of a bypass capacitor in a multi-layer board with solid power and ground planes.

Parasitic Pads. EDN (8/17/2000).
[REFLECTIONS] It seems that the very short 1-in. trace I'm using is covered more with part pads than with 50-ohm trace.

Passivation and Solder Mask. EDN (6/13/2002).
[ATTENUATION, MICROSTRIP, SKIN EFFECT] Copper traces on outer layers must be protected from corrosion by passivation or by coating them with an inert material.

Path of RF Current. HSDD Seminar (2015): 1.82.
[INDUCTANCE, RETURNING SIGNAL CURRENT, SILAB HSDD] Experiments at 1 and 10 MHz demonstrate the effect of circuit layout on the flow of current. (11 min.)

PCB Connectors. HSSP Seminar (2015): 5.26-5.41.
[CONNECTORS, CROSSTALK, EMC, REFLECTIONS] Measuring Signal Fidelity. Measuring Crosstalk. Measuring Ground-Transfer Impedance (EMI). Examples of Backplane Connectors. ERmetZD, I-Trac. RF Connectors. Concept of Tapered Transitions. Practical Co-planar Waveguide Taper. Nearly Co-planar Waveguide (NPW) Taper. Simple Taper Example. RF Connector Sizes. RF Connector Comparison. (28 min.)

PCB Traces at RF. HSNG Seminar (2015): 6.12.
[CROSSTALK, EXAMPLES, MIXED SIGNALS, SILAB HSNG] Mixed-Signal Isolation: Part III "PCB Traces": Showing two traces on the same side of the same board, and what it takes to attain 120 dB isolation between the two traces. Effects of grounding, good connector layout, and shielding. (20 min.)

PCI Bus. Newsletter v2-28 (10/22/1998).
[PCI] Discussion of "second-reflected-wave switching" and terminations.

PCI Series Terminations Resistors. Newsletter v1-4 (7/4/1997).
[DELAY, MULTI DROP, PCI] It's OK to use series termination resistors with bi-directional transceivers. The series resistor just delays the incoming signals and degrades their risetimes.

PECL Biasing. Newsletter v1-5 (7/14/1997).
[DIFFERENTIAL SIGNALING, TERMINATION] I thought that PECL outputs always need external resistors to ground since PECL drivers can only source current but not sink it.

Perfect Probe. EDN (10/14/2004).
[PROBES] The probe I want shows me exactly the signals I need to see without affecting signal quality when I touch the system.

Periodic Jitter. HSNG Seminar (2015): 5.69-5.89.
[EXAMPLES, JITTER] National Semiconductor EVK board. Main Types of Jitter. Jitter Test Setup. Jitter Track. Jitter Histogram. Synchronizing the scope with power supply ripple. Sync with AUX (waveform). Sync with VCC01 (waveform). Sync with FM mod (waveform). (25 min.)

Persistent Edge. Newsletter v8_05 (8/23/2005).
[RETURNING SIGNAL CURRENT, RISE TIME] Are there really any high-frequency currents still flowing in portions of a transmission line after those portions have been passed over by a voltage disturbance moving down the line?

Perspective and Vertical Height. HSNG Seminar (2015): 3.37-3.46.
[CONNECTORS, EMC, LAYOUT] Enchanted Rock (story). Example: Marshall LCD-15 Video Monitor. Consequences of stacking connector. (13 min.)

Picket Fences. W. Michael King. Newsletter v2-16 (6/8/1998).
[EMC, GROUNDING] About the use of a "picket fence" array of ground vias to shield internal sections of a board from each other.

Placement of End Termination. Newsletter v2-7 (2/25/1998).
[LAYOUT, TERMINATION] The sequencing of the end-terminator and its associated load can make a measurable difference in signal quality.

Planning For Signal Integrity. ED (5/12/1997).
[RINGING, SIMULATION] At these extremes of speed, even simple problems, like ringing, can become complex. Check out the nifty new simulation tools now available for dealing with signal integrity problems.

PLL Response Time. Newsletter v15_04 (12/10/2012).
[JITTER, RISE TIME] If you wish to clean up a jittery reference clock, removing the jitter, use a very low PLL tracking bandwidth. On the other hand, a serial data recovery application requires the highest PLL tracking bandwidth practicable.

Pointy Tips. EDN (5/29/2008).
[PROBES, TESTING] Some high-speed oscilloscope probes comes equipped with tips so pointy, so sharp, that you can set them down onto a pcb trace just as gently as a phonograph needle and still pick up a great signal.

Popsicle-stick Analysis. EDN (3/7/2002).
[PROXIMITY EFFECT, SIMULATION, SKIN EFFECT, TRANSMISSION LINE] You can model the proximity effect (and see edge-current concentration) using a simple model made from a sheet of rubber and a popsicle stick.

Potholes. EDN (11/11/1999).
[REFLECTIONS] Adjustments to the width of a transmission line on either side of a heavy capacitive load can partially compensate for the load.

Potholes (Transmission Line Imperfections). HSSP Seminar (2015): 5.16-5.25.
[CAPACITANCE, INDUCTANCE, REFLECTIONS, TRANSMISSION LINE] Reflection from a Capacitor. Reflection from a Short Hi-Z Segment. Compensation Idea. Example: Compensated Capacitance. Design Goal: Balance L and C. Limits to Applicability. (19 min.)

Power and Ground Resonance. EDN (9/1/1998).
[POWER SYSTEMS] (originally titled: Power Plane Resonance) Your power and ground planes do not form a perfect lumped-element capacitor.

Power Bus Noise. Newsletter v1-9 (8/26/1997).
[POWER DISSIPATION, POWER SYSTEMS] The CMOS devices that we have looked at can draw peak currents of about an Amp from the power bus (when a single gate switches) if they are connected with a sufficiently low inductance.

Power of Attraction. Newsletter v14_01 (2/11/2011).
[EM FIELDS, RETURNING SIGNAL CURRENT] Suspend a nickel in the air above the battleship Arizona. Remove all the conduction-band electrons from the nickel and place them on the battleship.

Power Plane Resistance. EDN (7/11/2002).
[POWER SYSTEMS, PROBES] The DC resistance between any two points within a region of arbitrary shape is easily measured.

Power Plane Resonance. EDN (9/1/1998).
[POWER SYSTEMS] Your power and ground planes do not form a perfect lumped-element capacitor.

Power Plane Segments. HSNG Seminar (2015): 3.48-3.51.
[FERRITE BEADS, LAYOUT, POWER SYSTEMS] When to Segment the VCC Plane. Power Region Placement. About Ferrite Beads. Information Required to "Design" Power Filter Network. (22 min.)

Power-Ground Source Impedance. Newsletter v2-4 (1/30/1998).
[POWER SYSTEMS] This reader takes issue with my claim of having achieved a power-to-ground impedance of 0.01 ohms by paralleling one hundred 0.1uF caps, each having 1 ohm or less impedance at the frequencies of interest.

Power-On-Reset. EDN (12/3/1998).
[POWER SYSTEMS] Many digital-design teams assign the design of the power-on-reset circuit to their youngest, least experienced engineer. This assignment is a mistake.

Practical Advice. EDN (11/22/2001).
[MANAGEMENT, TESTING] Years ago, an engineer named Allen Goodrich gave me a unique piece of advice.

Probe Ground Wire. HSDD Seminar (2015): 3.14-3.17.
[INDUCTANCE, PROBES] Sensitivity to Length of Ground Wire. Using Short Ground Attachments. (8 min.)

Probe Rise Time and Bandwidth. HSDD Seminar (2015): 3.10-3.13.
[BANDWIDTH, PROBES] Combining Probe and Scope Bandwidths. Example Calculations. (14 min.)

Probes. Newsletter v1-13 (10/6/1997).
[PROBES] How to accurately probe for noise on power supply nodes.

Probing for Noise. EDN (12/4/1997).
[PROBES] How can a probe pick up noise when looking at its own ground?

Probing High-Speed Digital Designs. ED (3/17/1997).
[PROBES] In high-speed system developments, the ubiquitous 10-pF 10:1 capacitive-input probe is no longer adequate. The two alternatives are the FET-input probe and the resistive-input probe.

Probing Two Points. Newsletter v5-12 (9/18/2002).
[FERRITE BEADS, PROBES] You should ground each probe near its respective point of measurement.

Properties of Gates. HSDD Seminar (2015): 2.1-2.10.
[GROUND BOUNCE] Voltage Margin Budget. SSO Noise (Ground Bounce). SSO Test Setup. Theory of Operation. How SSO Noise Affects Inputs. (23 min.)

Proximity Effect. Newsletter v4-1 (3/10/2000).
[PROXIMITY EFFECT, RETURNING SIGNAL CURRENT, SKIN EFFECT] Is there a "Proximity Effect" in strip lines or microstrips that is caused by currents flowing in adjacent conductors?

Proximity Effect II. Newsletter v4-3 (6/1/2001).
[PROXIMITY EFFECT, RETURNING SIGNAL CURRENT, SKIN EFFECT] Do you have any references dealing… with the current density distribution in a ground plane under a high frequency signal trace?

Proximity Effect III. Newsletter v4-8 (10/3/2001).
[CROSSTALK, HIGH-SPEED DESIGN FORMULAS, PROXIMITY EFFECT, RETURNING SIGNAL CURRENT] Justification for crosstalk approximation (see High-Speed Digital Design p. 190, eqn. [5.1])

Point to Point Wiring and Big Loads. Newsletter v3-16 (7/21/1999).
[REFLECTIONS, RINGING, WIRE WRAP] Your best choices are to either slow down the driver risetime a little bit so the whole thing acts as one big lumped-element circuit, or use a real 75-ohm transmission line.

Pulse Width Compression. EDN (3/29/2007).
[BANDWIDTH, TESTING] A pulse-width compression test overcomes the limitations of probe placement and loading.

Purpose of Differential Signaling. HSSP Seminar (2015): 6.1-6.11.
[DIFFERENTIAL SIGNALING, EE BASICS] Defeating Ground Bounce. Comparison of UTP and PCB Differential Applications. Differential Geometry on PCB. Distribution of Current in Edge-Coupled Microstrip. Differential Vocabulary. Modes of Propagation. Effect of Asymmetry. Vocabulary: Differential Peak-to-Peak Voltage. (30 min.)

Purpose of Simulation. HSSP Seminar (2015): 1.10-1.14.
[MANAGEMENT, SIMULATION] Must We Simulate Everything?. How Advanced Design Really Works. What You'll Need. (7 min.)

Quadrature Connector Layout. EDN (1/5/2012).
[CONNECTORS, CROSSTALK, EM FIELDS] Figure 1 illustrates the blueprint for a differential connector that radically reduces crosstalk between nearest-neighbor pairs.

Quadrature Via Layout. EDN (12/1/2011).
[CROSSTALK, EM FIELDS, VIAS] No matter where you place a differential via pair, you can always rotate its alignment to mitigate crosstalk from a troublesome differential source.

Quality. EDN (11/3/2011).
[MANAGEMENT] Quality is not the result of comprehensive computer simulations. Quality is the result of knowing, through experience, how a product will actually be used in the field and anticipating those needs.

Quality Factor. EDN (12/5/2005).

[BYPASS CAPACITORS] High-Q capacitors exacerbate resonances in a circuit, and resonance is the last thing you need in a power distribution system. Digital folks want low-Q capacitors.

Quantization Noise. Newsletter v9_02 (1/12/2006).
[SAMPLED DATA, TESTING] Measurement of low-level analog distortion requires two complementary things: a very good source and a very good instrument for signal detection.

Radiated Digital Ground Noise. Newsletter v2-17 (6/26/1998).
[EMC, GROUNDING] Ideally, you should ground your digital logic, the chassis, any cable grounds, and the cable shield (if present) to a common point.

Rainy-day Fun. EDN (3/4/1999).
[TRANSMISSION LINE] You can use puddles of water to solve certain difficult problems in the design of high-speed transmission lines.

Random and Deterministic Jitter. EDN (6/27/2002).
[CLOCKS, JITTER] The point of separating jitter into random and deterministic components is that the deterministic components have a lower ratio of peak value to standard deviation than do the random components.

RC Region. HSSP Seminar (2015): 3.15-3.20.
[ATTENUATION, RESISTANCE, TRANSMISSION LINE] Elmore Delay Estimation. Elmore Delay for Cascade of RC Networks. On-chip: Long-Haul Distribution. (6 min.)

Real Signals. EDN (10/8/2009).
[BANDWIDTH, RISE TIME] The step responses of high-speed digital drivers tend to look Gaussian. The same goes for scope probes and pre-amplifiers.

(The) Real Truth About Crosstalk. ED (8/18/1997).
[CROSSTALK, LAYOUT] If you are trying to manage crosstalk from first principles, so it comes out right on the first spin, look into the new crosstalk prediction tools that feature IBIS I/O modeling.

Really Cool Bus. EDN (10/26/2000).
[LAYOUT, MULTI DROP, TERMINATION] This unidirectional structure supports one driver with many, many loads.

Reason for Ground Split. Newsletter v9_04 (3/24/2006).
[CROSSTALK, GROUNDING, SPLIT PLANES] There are indeed applications so sensitive that they require separation of the analog and digital ground regions.

Reducing EMI with Differential Signaling. EDN (12/12/2002).
[DIFFERENTIAL SIGNALING, EMC] You need not struggle to place ordinary differential digital traces any closer than 0.5 mm for any EMI purpose.

Reducing EMI with Differential Signaling. HSSP Seminar (2015): 6.24-6.25.
[DIFFERENTIAL SIGNALING, EMC, EXAMPLES] Analysis of When Tight Trace Spacing Might Affect Signal Radiation. (5 min.)

Reducing Emissions. Bruce Archambeault. EDN (3/1/2001).
[EMC, TERMINATION] Most radiated emissions problems depend more on signal currents than signal voltages. The source-termination resistance controls both received signal amplitude and drive current.

Reference-Free Pair. EDN (7/20/2006).
[CHARACTERISTIC IMPEDANCE, DIFFERENTIAL SIGNALING] An "image plane" method calculates the impedance of an over/under configuration with no solid reference plane.

Reflections. HSDD Seminar (2015): 4.18-4.19.
[REFLECTIONS, TRANSMISSION LINE] Reflection Function. Reflection Chart. (11 min.)

Relevance of Physics. EDN (5/1/2003).
[ELECTROMIGRATION, MANAGEMENT, POWER DISSIPATION] The engineering curriculum for first-year students at Oxford University still includes a good amount of basic physics, despite attempts by computer scientists at other universities to de-emphasize that subject.

Remembrance. Newsletter v15_01 (2/28/2012).
[MANAGEMENT] On Jan 9, 2012, my father passed away at the age of 79 after a long battle with Alzheimer's…

Resistance. Newsletter v1-11 (9/15/1997).
[HIGH-SPEED DESIGN FORMULAS, POWER SYSTEMS] Regarding page 414, equation for calculating the DC resistance of power planes based on the diameters of two contact points space at X amount of distance.

Resistive Effects. HSSP Seminar (2015): 2.12-2.30.
[ATTENUATION, SKIN EFFECT, TRANSMISSION LINE] DC Series Resistance. DC Shunt Conductance. How Magnetic Shielding Works. The Walls of a Conductor Form a Shield. Skin Depth vs. Frequency for Copper. The Distribution of Current Changes With Frequency. High-Frequency Current Flows Only in a Shallow Band of Effective Depth d. High-Frequency Magnetic Fields. Paradox: Two Round, Symmetric Conductors. Proximity Effect. Popsicle-Stick Analysis. Proximity Effect for Differential Pcb Traces. Surface Roughness. Onset of Roughness Effect. Complete Resistance Model. (39 min.)

Resonance in Short Transmission Line. Newsletter v6-06 (4/14/2003).
[RINGING, TERMINATION] The resonant frequency and Q of a short, unterminated line varies strongly with capacitive loading.

Return Current in Plane. Newsletter v3-11 (4/26/1999).
[RETURNING SIGNAL CURRENT] Distribution of return current on the solid plane underlying a high-speed signal trace.

Return Current Matters. EDN (9/16/2004).
[DIFFERENTIAL SIGNALING, RETURNING SIGNAL CURRENT] Differential architectures sometimes tempt us to ignore return current issues… [but] even in a differential configuration, current flows on the planes under each trace separately.

Returning Signal Current at AF versus RF. HSNG Seminar (2015): 3.1-3.4.
[REFERENCE PLANES, RETURNING SIGNAL CURRENT] Distribution of High-Frequency Current Underneath a Signal Trace. (9 min.)

Review of Mathematical Fundamentals. HSSP Seminar (2015): 1.16-1.20.
[BANDWIDTH, EE BASICS, EM FIELDS, RISE TIME] Impedance and Bandwidth. Power Spectral Density of Digital Signal. 3-D Rule of Scaling—Lossless Circuits. 2-D Scaling of PCB Cross-Section. (25 min.)

RF Cables. HSNG Seminar (2015): 4.58.
[CROSSTALK, EXAMPLES, MIXED SIGNALS, SILAB HSNG] Mixed-Signal Isolation: Part II (continued): Measured crosstalk between two coaxial cables. (9 min.)

Ribbon Cable Impedance. Newsletter v3-10 (4/6/1999).
[CABLES, DIFFERENTIAL SIGNALING] The impedance of flat-ribbon cable depends on the pattern of grounds.

Right-Angle Bends. HSDD Seminar (2015): 6.69-6.71.
[LAYOUT, REFLECTIONS, TRANSMISSION LINE] Common sense related to feature size and uniformity. (12

min.)

Ringing in a New Era. EDN (10/9/1997).
[RINGING, SIMULATION] From this day forward there is absolutely, completely, totally no longer any excuse whatsoever for system problems, glitches, data errors or other artifacts related to ringing in digital signals.

Risetime of Lossy Transmission Line. EDN (10/2/2003).
[CABLES, RISE TIME] The risetime of a long skin-effect limited cable scales with the square of its length, not according to the sum-of-squares rule for [the risetime of] cascaded linear systems.

Risetime with Reactive Load. HSDD Seminar (2015): 6.61-6.62.
[CAPACITANCE, CIRCUIT TOPOLOGY, INDUCTANCE, RISE TIME] Capacitive load effect on risetime. Inductive bead effect on risetime.

Rising Problem. Newsletter v9_05 (6/16/2006).
[BANDWIDTH, REFLECTIONS, RINGING] The Gaussian edge best represents actual digital logic. It displays virtually no perceptible ringing in the time domain—just like the real circuit

RoHS with Joe Fjelstad. HSNG Seminar (2015).
[RELIABILITY, SILAB HSNG, SOLDERING] Lead-free solder is not a "green" solution. Lead-free solder actually damages the environment more than 60/40 solder. System-reliability impact of lead-free solder. (21 min.)

Routing Clocks and Other High-Speed Signals. HSSP Seminar (2015): 12.1-12.14.
[CLOCKS, LAYOUT] Special Requirements for Clock. Clock Repeaters are Built to Provide Multiple Low-Skew Clocks. Active Skew Correction. Clock Tree. Zero-Delay Clock Repeater. Point to Remember. Stripline vs. Microstrip Delay. Delay of Typical Microstrips. Importance of Terminating Clock Lines. Ringing on Short, Un-terminated Trace Distorts Timing. Ground Bounce Effect on Clock. Crosstalk. Advice on Routing Differential Clocks. (23 min.)

Scattering Parameters. Newsletter v6_03 (2/17/2003).
[REFLECTIONS, SIMULATION] Relates S-parameter matrices provided by a network analyzer to transmission-matrices used for simulation work.

Scattering parameters (S-parameters). HSSP Seminar (2015): 4.10-4.20.
[S-PARAMETERS] S-Parameter Test Setup. Wafer Probe Design. Transmission Lines are Symmetric. Do Not Cascade S21 Terms. Do Not Multiply S-Matrices. Proper S-Matrix Combination. Conversions Between Forms. Using S-Parameters with Spice. Good Applications for S-Parameters. (27 min.)

Scope Probes and Loading. HSDD Seminar (2015): 3.1-3.9.
[CAPACITANCE, PROBES] FET-input probe. Differential Active Probe. Resistive-input probe. Input Impedance of Probes. Effect of Probe on Signal Under Test. Which Probe is Best? (13 min.)

Scrambled Bus. Newsletter v7_10 (12/14/2004).
[DATA CODING, EMC] The improvement in common-mode radiation from the straight, unencoded, worst-case example to the best scrambled-and-coded version is better than 30 dB.

Scrape It. EDN (5/1/2008).
[MICROSTRIP, PROBES] I only know six ways to remove solder mask for probing: Scraping, milling, grinding, micro-blasting, chemical stripping, and ultraviolet (UV) illumination.

Second-Level Interconnects. Newsletter v2-15 (6/4/1998).
[INTERCONNECTIONS, SYSTEM-ON-A-CHIP] A reader suggests, "The days of discrete design and interconnect are rapidly disappearing, if not gone already."

See Beyond the Edge. EDN (10/13/2005).
[CHARACTERISTIC IMPEDANCE, S-PARAMETERS, TESTING] The far-end reflected signal is usually considered the end of usable data in a TDR waveform, but a wealth of information lies beyond this point.

Seek Inspiration. EDN (6/25/2013).
[MANAGEMENT] Successful engineers purposefully drive their career in the direction they want it to go. They meet a lot of people. They seek inspiration.

Segmenting the VCC Plane. HSDD Seminar (2015): 5.53-5.54.
[LAYOUT, POWER SYSTEMS, SPLIT PLANES] When to do it.

Segmenting the Vcc Plane. Newsletter v2-18 (7/23/1998).
[EMC, FERRITE BEADS, POWER SYSTEMS] I don't cut up the Vcc plane unless I have one circuit that is substantially more sensitive to Vcc noise than the other circuits on the board.

Serial Killers. Newsletter v7_07 (12/1/2004).
[DATA CODING, SERIAL LINK] If you are responsible for selecting a serial interface standard, I'd like to pass along a few ideas for your selection criteria, starting with some concepts having to do with the physical link protocol, particularly DC balance.

Serial Link Architecture. HSSP Seminar (2015).
[CROSSTALK, DIFFERENTIAL SIGNALING, EXAMPLES, LAYOUT, SILAB HSSP] Example of 10Gbps Serial Link. Introduction to System Modelling. Trace Layout. Crosstalk from Various Sources. (31 min.)

Serial Link Budgeting. HSSP Seminar (2015).
[ATTENUATION, BACK PLANE, DIFFERENTIAL SIGNALING, DISPERSION, EXAMPLES, REFLECTIONS, SILAB HSSP] A Simple Signal Quality Budget. Discussion of PCB Transitions. Backdrilling. PCB Trace Losses. Signal Dispersion and the Effect of Equalization. (43 min.)

Series Resonance. EDN (3/1/2012).
[EE BASICS, POWER SYSTEMS] A digital power system needs lots of large, simple, non-resonant, bypass capacitors, not fancy resonant circuit tricks.

Series Termination (Source Termination). HSDD Seminar (2015): 6.16-6.27.
[CIRCUIT TOPOLOGY, TERMINATION] Halving and Doubling of Signal Amplitude. Value of External Series Resistor. No Clock Receivers Allowed in Middle of Series-Terminated Line. What's That Plateau?. What's That Glitch?. Heavy Capacitive Loads on Series and End-Terminated Lines. How Close Must a Series-Terminator Be to the Driver? (27 min.)

Serpentine Delays. EDN (2/15/2001).
[CLOCKS, DELAY, SKEW] If you are using some form of delay line to match clock delays at all points of usage within a pc board, here's a short list of the items you need to match:

Serpentine Traces. HSSP Seminar (2015): 12.15-12.19.
[CLOCKS, DELAY, LAYOUT] Serpentine Coupling. Coupled Serpentine Waveforms. 24-Section Serpentine. Rules for Successful Delay Lines. (13 min.)

Setting the Standard for Gigabit Ethernet. ED (6/23/1997).
[GIGABIT ETHERNET] The Gigabit Ethernet standard provides for a number of physical layer transmission interfaces.

Settling Time Measurements. Newsletter v3-17 (7/28/1999).
[DELAY] What is the correct method to measure the settling time of a digital waveform?

Seven Percent Solution. EDN (6/10/2010).
[TERMINATION, TESTING] The distribution of 10%-resistor values in a bin does not follow a simple Gaussian profile.

Severe Overshoot. Newsletter v2-31 (12/2/1998).
[OVERSHOOT, RINGING] Will overshoot and undershoot impact the receiver, damage it or cause excessive recovery time?

Severe Overshoot Mailbag. Newsletter v3-1 (1/14/1999).
[OVERSHOOT, RINGING] ...the clamp diodes shot current into the VCC net… …make sure you are measuring the overshoot correctly… ...Undershoot on some lines on some SRAM chips will cause "weak writes"…

Shannon Says. EDN (11/13/2003).
[CONNECTORS, CROSSTALK, MULTI LEVEL] Connector vendors will soon realize that great improvements in the information-carrying capacity of their products may be had by reducing crosstalk.

Shaping Edges. EDN (11/12/2009).
[RISE TIME, SAMPLED DATA] If you have a record of a driver's actual output signal shape, or can extracted it from an IBIS file, use it. In the absence of other information, assume a Gaussian shape.

Sharp Edges. EDN (6/22/2006).
[RINGING, SIMULATION] A PWL edge over-stimulates the resonant behavior. A smooth Gaussian edge better represents a real digital signal, eliminating phantom ripples in your simulation output.

Short Transmission Line Model. Newsletter v3-18 (8/7/1999).
[TRANSMISSION LINE] Lumped-element modeling of transmission line behavior using the "PI-Model"

Short-Term Impedance of Planes. Newsletter v6_05 (3/24/2003).
[EM FIELDS, POWER SYSTEMS, RETURNING SIGNAL CURRENT, VIAS] Doesn't the returning signal current just pop between the planes through the parasitic capacitance of the planes themselves, you might ask?

Shot Heard 'Round the World. EDN (10/16/2008).
[REFLECTIONS, RINGING, TERMINATION] Let's apply Sabine's theory of acoustic reverberation to a digital problem.

Signal Ground Drain Wire. Newsletter v2-32 (12/4/1998).
[CABLES, CONNECTORS, EMC, GROUND BOUNCE] Why should disconnecting the "drain wire" at the connectors have such a drastic impact on the rise/fall time of the outer conductors?

Signal Integrity Mailbag. EDN (10/8/1998).
[CLOCKS, EMC, JITTER] My recent column on intentional clock modulation (EDN, Aug 3, 1998, pg 24) spurred some interesting responses from readers.

Simulation Software. Newsletter v1-16 (11/4/1997).
[EMC, SIMULATION] What are the primary issues at hand, and what are the important questions to ask before you get yourself mired in a project that may not pay off.

Single Point Ground. Newsletter v2-26 (9/29/1998).
[GROUNDING] Moat-and-drawbridge approach used on mixed-signal board.

Skin and Dielectric Loss Chart. HSDD Seminar (2015): 1.84-1.85.
[DIELECTRIC LOSS, SKIN EFFECT] Fibre Channel example at 1.06 Gb/s over 18 in. of FR-4 PCB trace.

Skin Effect Calculations. Web.
[SKIN EFFECT] Derivation of skin-effect loss equations in High-Speed Digital Design

Skin Hot. EDN (3/6/2003).
[SKIN EFFECT] How skin resistance changes with temperature.

Skin-Effect Region. HSSP Seminar (2015): 3.21-3.25.
[ATTENUATION, SKIN EFFECT, TRANSMISSION LINE] Random Test Patterns. Effective Settling Time. Pretty-

Bad Test Pattern. (12 min.)

Sliding Edge. EDN (9/3/2009).
[REFLECTIONS, TRANSMISSION LINE] When you connect two boards made from dissimilar fiberglass laminate materials, will high-speed signals reflect due to the sudden change in board properties as they move across the connection interface?

Slippery Slopes. EDN (4/1/2004).
[DIFFERENTIAL SIGNALING, SKEW] Differential Skew revisited: skew disperses your risetime, increasing your susceptibility to jitter caused by additive noise.

Slow Wave Mode. EDN (11/8/2001).
[DELAY, TRANSMISSION LINE] The slow-wave effect hampers signal transmission on some on-chip MIS (metal-insulator-semiconductor) interconnections.

So Good it Works on Barbed Wire. EDN (7/5/2001).
[CABLES, TRANSMISSION LINE] Next time you look at a transmission line, I hope you'll focus on the big four properties: characteristic impedance, high-frequency loss, delay, and crosstalk.

Software Crosstalk. Newsletter v5-0 (6/24/2002).
[CROSSTALK] Explains why software tests for ringing and crosstalk are necessary and what specific features are needed.

SONET data coding. Newsletter v5-5 (3/29/2002).
[DATA CODING, LEVEL TRANSLATION] Figure 1 shows one way to build a non-linear DC restorer. This circuit fixes the DC balance of a SONET data string that has lost its DC level because of AC-coupling.

(The) Sound of Progress. EDN (5/12/2011).
[BACK PLANE, CONNECTORS] The vias and breakout patterns underneath a connector control its physical scale and thus its electrical performance.

Source-Terminated Bus Structures. HSDD Seminar (2015): 6.53-6.57.
[MULTI DROP, TERMINATION, TRANSMISSION LINE] PCI-Bus (ver. 2.1, 1995). Compromises in Design. Circle Bus. (10 min.)

Space-Time Diagrams. Newsletter v12_02 (1/25/2009).
[BACK PLANE, TRANSMISSION LINE] Where the waves cross, at each point in time and space the transmission line sums their amplitudes. Like rogue waves crossing in the middle of the ocean, the effective total height of the combination may exceed that of either wave alone.

Specsmanship. EDN (2/2/2006).
[MANAGEMENT] Every Joe at the lumberyard understands that a 2x4 does not measure two inches by four inches.

Split Power Planes. HSDD Seminar (2015): 5.43-5.46.
[CROSSTALK, LAYOUT, POWER SYSTEMS, SPLIT PLANES] Crossing a Split Power Plane Boundary. Use of Stitching Capacitors. Measuring Split-Plane Crosstalk. (8 min.)

Spotlight Interview with Dr. Howard Johnson. Web (2/21/2012).
[MANAGEMENT] Dr. Johnson responds to questions from the EE Web staff about technology, it's direction, the importance of early education, and the influence of parents and mentors. This article is reprinted in honor of his father, Dr. Jim Johnson, 1932-2012.

Spread Your Returns. EDN (3/31/2005).
[CROSSTALK, GROUND BOUNCE] BGA package analysis; Signals closest to a good return suffer the least ground bounce.

Spurious Magnetic Interference. HSDD Seminar (2015): 3.18-3.25.

[CROSSTALK, PROBES] Measuring Your Noise Floor. Probe Shield Currents. Differential Probing. Probing Without Ground. (12 min.)

Squeeze Your Layer Stack. Newsletter v7_04 (9/1/2004).
[BACK PLANE, DIELECTRIC LOSS, VIAS] Given the same trace width and trace impedance, a lower dielectric constant lets you squeeze the layer stack.

SSO (Ground Bounce). HSNG Seminar (2015): 2.23-2.25.
[CHIP PACKAGING, CROSSTALK, GROUND BOUNCE] SSO Test Setup and theory (introduction to movie). (10 min.)

Star Topology. EDN (11/11/2004).
[RINGING, TERMINATION] A star topology connects N devices in a completely symmetrical, peer-to-peer fashion.

Steel-plated Power Planes. EDN (3/21/2002).
[POWER SYSTEMS, REFERENCE PLANES] A thin coating of steel, applied to the inside-facing surfaces of a power and ground plane pair may help damp power plane resonance.

Step Response Test. Newsletter v11_01 (3/13/2008).
[CONNECTORS, PROBES, TESTING] My favorite repetitive step response stimulus is a simple square wave with 50% duty cycle. (This article includes many details of measurement technique and interpretation.)

Straddle-Mount Connectors. Newsletter v4-18 (12/19/2001).
[CHIP PACKAGING, CONNECTORS] Follow-up to "Tapered Transitions", EDN 11 Oct., 2001

Strange Microstrip Mailbag. Newsletter v4-16 (11/28/2001).
[DISPERSION, MICROSTRIP, TRANSMISSION LINE] Follow-up to April 26, 2001 column in EDN, "Strange Microstrip Modes."

Strange Microstrip Modes. EDN (4/26/2001).
[BANDWIDTH, OVERSHOOT, TEM MODE, TRANSMISSION LINE] "Quasistatic" values of capacitance and inductance are the values you get at low frequencies, near dc.

Stripline Crosstalk Study. HSDD Seminar (2015): 5.18-5.20.
[CROSSTALK, LAYOUT, STRIPLINE] Modeling crosstalk using the D/H ratio.

Stub Termination. Lambert (Bert) Simonovich. EDN (5/13/2010).
[TERMINATION, VIAS] A via-stub termination can eliminate via resonance at the expense of a modest amount of flat-loss attenuation.

Stubs & Vias. Newsletter v2-25 (9/16/1998).
[REFLECTIONS] I would like to know the effects of stubs and vias in high-speed PCB designs.

Submicron ASICs and EMI-EMC. EDN (4/13/2000).
[CHIP PACKAGING, EMC] Above Fk the limited rise/fall time in your chips provides a natural filtering effect that limits emissions.

Superposition. EDN (10/7/2010).
[EE BASICS] Linear superposition opens the door to many advanced methods of circuit analysis.

Surface Roughness. EDN (12/6/2001).
[ATTENUATION, SURFACE ROUGHNESS, TRANSMISSION LINE] At a microscopic scale, no surface appears perfectly smooth.

Synchronizing clocks. Newsletter v4-6 (6/19/2001).
[CLOCKS, SKEW, SYNCHRONIZATION] What should I do to prevent noise problems if I choose not to synchronize the whole clock tree.

System Test. HSNG Seminar (2015): 7.1-7.13.
[TESTING] Compliance Testing vs. Debugging. An Eye Pattern is a Compliance Test. Example: 2.5 Gb/s Differential Link. Compilation of Eye Diagram. Worst Patterns are Clearly Visible Within the Eye. A Step Response is a Debugging Test. Compliance Testing: Interview with J. P. Miller. Debugging Procedures. Working with Very Pure Signals: SINAD. Working with Very Large Signals: ESD. (28 min.)

System-Level Grounding. HSNG Seminar (2015): 4.64-4.72.
[CROSSTALK, GROUNDING] Earth Potential. Building Wiring. Rules for System-Level Grounding. (17 min.)

Take the Fifth. EDN (2/3/2011).
[EE BASICS, RISE TIME] How many harmonic terms must I take to adequately represent a good squarewave?

Tapered Transitions. EDN (10/11/2001).
[CHARACTERISTIC IMPEDANCE, CONNECTORS] Consider the problem of adapting a straddle-mount SMA connector for a 10-Gbps digital application.

TDR and Ice Cube Trays. Newsletter v3-5 (2/5/1999).
[RETURNING SIGNAL CURRENT, TRANSMISSION LINE] The "Ice Cube Tray" model of distributed transmission.

TEM Transmission Media. HSSP Seminar (2015): 3.1-3.7.
[DISPERSION, NON-TEM, TRANSMISSION LINE] Attenuation vs. Frequency (graph). Characteristic Impedance (graph). Approach to Modeling. General Properties. Is a Transmission Line Ever Not a Transmission Line? (demonstration). (15 min.)

Ten Layer Stack. Newsletter v2-11 (4/27/1998).
[LAYER STACK, RETURNING SIGNAL CURRENT] Discussion of multi-layer board stack for system with multiple power voltages.

Ten Measurements. EDN (5/10/2012).
[TESTING] Ten measurements define the body of knowledge we call, "Signal Integrity." Master them, and you will become a guru of the art.

Terminator Crazy. ED (10/1/1996).
[RETURNING SIGNAL CURRENT, TERMINATION] The first clue as to whether a terminator is needed is the ratio of trace delay to rise time.

Terminator I. EDN (3/2/2006).
[REFLECTIONS, RISE TIME, TERMINATION] If you can limit the magnitude of the reflections to, say, x percent of the signal swing, then the worst-case time-domain jitter induced by those errant reflected blips will amount to only a x percent of the signal risetime.

Terminator II. EDN (3/30/2006).
[REFLECTIONS, RISE TIME, TERMINATION] Resistor R2 acts as an isolation component, preventing the FPGA capacitance from directly loading the terminating resistor.

Terminator III. EDN (4/27/2006).
[REFLECTIONS, RISE TIME, TERMINATION] I want to force the apparent termination impedance to equal precisely 50 ohms, with minimum degradation of the received signal risetime.

The Path of Returning Signal Current. HSDD Seminar (2015): 5.12-5.17.
[REFERENCE PLANES, RETURNING SIGNAL CURRENT, TRANSMISSION LINE] The High-Speed Path Can Look Pretty Strange. Distribution of High-Frequency Current Underneath a Signal Trace. What about Capacitance?. Crosstalk Versus Trace Separation Experiment. Crosstalk Over a Solid Ground Plane (waveforms). Crosstalk Over a Solid Ground Plane (graph). (21 min.)

Think Small. Newsletter v8_04 (5/4/2005).
[CHIP PACKAGING, EM FIELDS, RISE TIME] The three-dimensional rule for physical scaling of electrical connections immutably controls the performance of connectors, packages, component bodies, vias, and many other common structures.

Three Drop Bus. Newsletter v4-12 (10/18/2001).
[LAYOUT, MULTI DROP, POWER DISSIPATION] The three privileged locations on a long net are at one end, the other end, and right smack in the middle.

Three Ideas for Audio-Frequency Isolation. HSNG Seminar (2015): 4.14-4.22.
[CROSSTALK, GROUNDING, MIXED SIGNALS, SPLIT PLANES] High Impedance Blocks Unwanted Current. Low Impedance Shunts Current Away. Change the Topology. Example: ADC Grounding. Moats for Multiple ADCs. Align Each Moat with Its Special Power Region. Moats and Floats: Your Chance to Experiment. (27 min.)

Through-hole Clearances. EDN (7/8/1999).
[CONNECTORS, CROSSTALK, ERNIE] Connectors require continuity of the ground plane underneath the connector.

Tight Coupling. HSDD Seminar (2015): 6.68.
[DIFFERENTIAL SIGNALING, LAYOUT] Summary of effects (good and bad).

Time Invariance. EDN (11/4/2010).
[EE BASICS] Hard clipping obeys time-invariance, but not superposition. A tremolo circuit obeys superposition, but varies its gain with time.

Tiny Difference. Newsletter v9_08 (12/21/2006).
[LAYOUT, PROBES, SKEW] Measuring a tiny time difference like 5 ps can be quite challenging. Anjaly will need well-matched, skew-calibrated probes and perfectly symmetric attachments to the board.

Tips on Controlling Clock Skew. ED (7/21/1997).
[CLOCKS, SKEW] Your ability to manage and control clock skew has been recently improved by the introduction of a new generation of multi-output, low-skew clock drivers.

To Tee or Not To Tee?. EDN (2/2/1998).
[LAYOUT, MULTI DROP] The basic problem with this topology is that all three branches are long compared to the length of a rising edge.

Tools for Highly Optimized Work Above 1 GHz. HSSP Seminar (2015): 1.15.
[MANAGEMENT, PROBES, TESTING] Scope and probes. Vector network analyzer. Budget and time for multiple board spins. Ringing and Crosstalk (2D) simulator. Full-wave (3D) simulator. Power integrity simulation. (9 min.)

(The) Torches and the Hair. DesignCon 2003 (2/17/2003).
[BANDWIDTH, MULTI LEVEL, SERIAL LINK] Mankind has a long history of experience dealing with bandwidth-limited communication channels.

Trace Between Capacitors. Newsletter v3-4 (1/28/1999).
[CROSSTALK, LAYOUT] Will crosstalk occur if I route a trace underneath a bypass capacitor?

Trace Inductance. Newsletter v3-8 (3/23/1999).
[TRANSMISSION LINE] Can you give me a basic (approximate) formula for the inductance of (1) a bare pc trace, and (2) A trace suspended above an adjacent plane.

Trace Scaling. EDN (3/4/2010).
[SIMULATION, SKIN EFFECT] How to circumvent minimum feature-size limitations in your SI simulation tool.

Trace Width vs. Distance. HSSP Seminar (2015): 6.18-6.19.
[ATTENUATION, LAYOUT, TRANSMISSION LINE] Summary of trace width effects. (2 min.)

Transmission Line Basics. HSSP Seminar (2015): 2.1-2.11.
[CHARACTERISTIC IMPEDANCE, TRANSMISSION LINE] Telegrapher's Model. RLGC Model. Meaning of "TEM" mode. Voltage and Current Waveforms on Lossless Line. Charges in Motion (animation). What happens after a Pulse "Leaves the Station?". (37 min.)

Transmission Lines. HSDD Seminar (2015): 4.1-4.3.
[EE BASICS, TRANSMISSION LINE] What Makes a Transmission Line?. Four Main Properties. (12 min.)

Transmission Lines/Gate Delay. Newsletter v1-19 (12/4/1997).
[TRANSMISSION LINE] What does this mean: "Until the driver becomes aware of the impedance mismatch at the end of the line the line looks resistive"

Transmission-line Scaling. EDN (2/4/1999).
[BANDWIDTH, TRANSMISSION LINE] Every pc-board trace has a limited bandwidth. As chips go faster and faster, you eventually run into this limitation.

Tricky DRAM Lines. Newsletter v1-20 (12/15/1997).
[LAYOUT, MULTI DROP, SPLIT PLANES] The app note I'm looking at suggests that my DRAM address lines run in a "T" shape… with a ground plane cut under the DRAMs

Twisted Crosstalk. Newsletter v12_01 (1/9/2009).
[CROSSTALK, EM FIELDS] Differential links have a good reputation for rejecting external noise. Unfortunately, that good reputation extends only to noise that affects both wires equally.

Twisted Impedance. EDN (9/18/2008).
[CHARACTERISTIC IMPEDANCE, DIFFERENTIAL SIGNALING] When separation, S, is less than wire diameter, D, doesn't your formula ln(2S/D) return a negative value for characteristic impedance? What gives?

Two-way Street. EDN (1/4/2007).
[PROBES, SIMULATION] Transmission lines, like streets, support traffic in two directions. A voltage probe shows only an aggregate voltage waveform, but doesn't say which way the waveform is moving.

Uncertainty Principle. EDN (7/19/2007).
[BANDWIDTH, RISE TIME, TESTING] The shorter the duration of an event in time, the wider must be the spread of frequencies associated with it.

Understanding Grounding. HSNG Seminar (2015): 4.1-4.13.
[CROSSTALK, GROUNDING, RETURNING SIGNAL CURRENT] Immutable Law of Development. Difficulties Understanding Orders of Magnitude. Difficulties Imagining Behavior of Solid Sheets of Copper. Picture Frame Analysis: a New Way of Thinking. Principle of Single-Point Grounding. A Common Grounding Mistake. Principle of Moat and Drawbridge Construction. Single-Point Connection to Chassis. Double-Connected Analog Region. But, I Did the Bad Thing and It Worked!. (12 min.)

Undo Machine. EDN (1/6/2011).
[EE BASICS, EQUALIZATION, SAMPLED DATA] The signal distortion caused by some linear time-invariant processes can be completely un-done.

Unexpected Synchronization Difficulties. HSNG Seminar (2015): 5.1-5.9.
[DATA CODING, DIFFERENTIAL SIGNALING] What Happens When You Unplug a Link?. How To Detect Unplugged or Inoperative Links. Well-Balanced Plug-able Differential Interface. Killer Packets.

Difficulties with Multi-synchronous Systems. (31 min.)

Unified Eletrodynamic Force. EDN (2/5/2009).
[EM FIELDS] The magnetic force is nothing more, and nothing less, than a direct consequence of Einstein's theory of relativity.

Un-terminated Line Examples. HSDD Seminar (2015): 4.20-4.30.
[CIRCUIT TOPOLOGY, OVERSHOOT, RINGING, TRANSMISSION LINE] Example: Source Impedance Too Low. Example: Source Impedance Too High. (22 min.)

Using Ferrites. Newsletter v1-2 (6/13/1997).
[CROSSTALK, FERRITE BEADS] If two or more ferrites are placed parallel and close to each other will this result in crosstalk between them?

Value of DC blocking capacitor. HSSP Seminar (2015): 6.50-6.53.
[DC BLOCK] Modeling DC baseline wander. Maximum wander varies with data coding.

Value of End Terminator. Newsletter v5-1 (1/7/2002).
[EMC, TERMINATION] Should an end-terminator always be set at the highest value that works because that minimizes the current and therefore gives the best EMI performance?

Via Capacitance. Newsletter v5-9 (7/15/2002).
[VIAS] Formula [7.6] in High-Speed Digital Design for the capacitance of a via is a crude approximation. I've now got some better material.

Via Geometry. HSSP Seminar (2015): 5.52-5.63.
[CHARACTERISTIC IMPEDANCE, LAYOUT, VIAS] Movie Quiz: Adjustments to Via Geometry. Shallow Blind Vias. Blind Via Capacitance (table). Inductance of Vias That Penetrate Multiple Planes. Via Inductance (example calculation). Stripping Via Pads on Unused Layers. Efficacy of Stripping Pads. (26 min.)

Via Inductance. Newsletter v6-04 (3/15/2003).
[EM FIELDS, HIGH-SPEED DESIGN FORMULAS, RETURNING SIGNAL CURRENT, VIAS] The inductance of a via depends on the path of returning signal current.

Via Inductance II. Newsletter v6_08 (9/10/2003).
[VIAS] Corroborates real-world measurements of via inductance with a simple approximation.

Via Reflections. HSDD Seminar (2015): 6.72-6.73.
[LAYOUT, REFLECTIONS, TRANSMISSION LINE] Treating the via as a lumped capacitance. Effect of short trace stubs.

Visible Return Current. Newsletter v8_08 (12/1/2005).
[RETURNING SIGNAL CURRENT] I may at last have found a way to demonstrate, in a direct (and dramatic) fashion, to any observer, where and how high-frequency current flows in a printed circuit board.

Visualizing Differential Crosstalk. EDN (12/5/2008).
[CROSSTALK, DIFFERENTIAL SIGNALING] The spacing between the wires of a differential stripline pair affects crosstalk only mildly

Visualizing Differential Crosstalk. HSSP Seminar (2015): 6.26-6.30.
[CROSSTALK, DIFFERENTIAL SIGNALING, EXAMPLES, STRIPLINE] Tight Coupling vs. Crosstalk. (7 min.)

Vocabulary. HSDD Seminar (2015): 1.11-1.27.
[CAPACITANCE, EE BASICS, INDUCTANCE] Your Schematic shows only the intended flow of signal power. Currents Form Loops. Every Loop of Current Has Inductance. Behavior of Inductance. Impedance

Magnitude of Inductor. Effect of Inductor. Importance of Returning Current Path. Proximate Conductors Share Capacitance. How Capacitors Behave. Impedance Magnitude of Capacitor. Effect of Capacitor. Approximate Values of Capacitance. Practical Circuits are Littered with Parasitic Elements. (38 min.)

Voltage Conversion. Newsletter v9_01 (1/4/2006).
[ATTENUATION, TERMINATION] James Buchanon points out that my attenuating terminator may be impossible!

Voltage Regulator Droop. EDN (9/14/2006).
[POWER SYSTEMS] When the load draws current, the new larger value of regulator output resistance will increase the droop measured at Vcc. That sounds bad, but in some very special circumstances it is actually good for your circuit.

Voltage Regulator Model. EDN (8/17/2006).
[BYPASS CAPACITORS, POWER SYSTEMS] One step-response test reveals enough information to form a simple circuit model of most any voltage regulator.

VRM Stability - Part I: Feedback. Newsletter v10_3 (9/10/2007).
[CROSSTALK, POWER SYSTEMS] Feedback must be carefully controlled because, by its very nature, feedback invites the risk of self-oscillation.

VRM Stability - Part II: ESR. Newsletter v10_4 (9/17/2007).
[BYPASS CAPACITORS, POWER SYSTEMS] The ESR of your VRM output capacitor controls both its ripple amplitude and stability.

Wafer-Probe Launch. EDN (10/6/2011).
[LAYOUT, TESTING] At 28-Gb/s the SMA runs out of gas, so connect your VNA to the layout test card using a high-performance microwave wafer probe.

Water Analogy. EDN (7/15/2010).
[EE BASICS] Pump A forces water at constant pressure p1 around a closed loop controlled by valve B at a steady velocity v1. This is the law of

Water Hammer. EDN (8/12/2010).
[EE BASICS, ERNIE] A system of water pipes with a large electric snap-action water valve and a flow regulator explodes at midnight.

Watery Grave. EDN (6/23/2005).
[ESD] Design your system to survive near-miss situations. The most common near-miss scenarios include discharges to your product chassis, the wires leading into or out of your chassis, or metallic objects near those wires.

(The) Way Home. EDN (6/22/2000).
[BYPASS CAPACITORS, LAYOUT] Current always makes a loop. If it goes out, it must find a way back home. The shapes of both the outgoing and the return paths affect the observed inductance.

Way Too Cool. EDN (2/4/2010).
[MANAGEMENT, POWER DISSIPATION] LED traffic lights clog with snow, become indiscernible, and cause fatal traffic accidents.

Weak End-Termination. HSDD Seminar (2015): 6.65.
[CIRCUIT TOPOLOGY, TERMINATION] Terminations do not have to be perfect. (1 min.)

Whang That Ruler. EDN (4/7/2011).
[RINGING, TERMINATION] A capacitive load applied to a pcb trace lowers its resonant frequency much like a quarter taped to the end of a ruler lowers its resonant pitch.

What is Jitter. HSNG Seminar (2015): 5.26-5.40.
[JITTER] Racing Game Analogy. Tracking Bandwidth. Definitions of Jitter. Jitter: a New Dimension. Why Jitter Matters. Causes of Jitter. Additive Noise. Vertical Shift vs. Timing Offset. Three Ways to Reduce Additive Jitter. Sources of Additive Noise. (21 min.)

What's Different at RF. HSNG Seminar (2015): 4.24-4.46.
[LAYOUT, MIXED SIGNALS] Overview of RF issues. Capacitance of planes. Inductance of wires. Structural resonance. Adequate grounding. (41 min.)

What's That Glitch?. EDN (8/19/2004).
[REFLECTIONS, TRANSMISSION LINE] Have you ever seen a non-monotonic glitch in a signal like the one shown in Figure 1? Can you guess what causes it?

What's That Plateau?. Newsletter v7_03 (6/14/2004).
[PROBES, TERMINATION, TRANSMISSION LINE] An unexpected plateau implies the presence of a transmission line stub.

When Everything Matters. EDN (1/6/2005).
[MANAGEMENT] Squeeze that last drop of performance from a CMOS architecture by turning up the clock or adding a few new features and you may choke on the curse of complexity—where every decision you make interacts with every other decision.

When Logic Switches Too Fast. ED (7/1/1996).
[RISE TIME] When new chips are substituted into older designs, the new, faster chips may bring you nothing but headaches.

When to use AC Coupling. Newsletter v4_15 (11/13/2001).
[CLOCKS, INTERCONNECTIONS, LEVEL TRANSLATION] When should one adopt DC coupling versus AC coupling?

Who's Afraid of the Big, Bad Bend?. EDN (5/11/2000).
[MICROSTRIP, REFLECTIONS, TRANSMISSION LINE] Right-angle bends in PC-board traces perform perfectly well in digital designs in speeds as fast as 2 Gbps.

Why 50-Ohms Mailbag. EDN (1/4/2001).
[CABLES] Regarding my article "Why 50 Ohms?" (EDN, Sept 14, 2000, pg 30), I received some interesting justifications for the use of 50-ohm coaxial cabling.

Why 50 Ohms?. EDN (9/14/2000).
[CABLES, TRANSMISSION LINE] Why do most engineers use 50-ohm pc-board transmission lines? Why not 60 or 70 ohms ?

Why Digital Engineers Don't Believe in EMC. EMC Soc nwsltr (3/2/1998).
[EMC] Digital engineers don't believe current flows in loops, existence of the H-field, gates are differential amplifiers, existence of EM waves, or that EMC will advance their careers

Why is That?. Newsletter v11_05 (9/2/2008).
[REFLECTIONS, TERMINATION] You need three things: Good measurement equipment, a simulation system handles your application, and knowledge of what factors might reasonably affect your design. I teach the knowledge part.

Why Johnny Can't Design a High-Speed Digital System. DesignCon 2003 (2/17/2003).
[MANAGEMENT] As a class, digital engineers are less well equipped now than they were 30 years ago to design a high-speed digital system.

Why Reflections Happen. EDN (5/22/2013).
[CHARACTERISTIC IMPEDANCE, REFLECTIONS, TERMINATION] Whatever impedance creates no reflection is DEFINED as the characteristic impedance of the transmission structure. There is no other definition.

Why Teach Science?. EDN (2/1/2007).
[MANAGEMENT] Science is not for everybody. You could live like an aborignal, running around naked in the forest chasing deer with bows and arrows, for all I care.

Winsome Waveform Wizardry. Web (1/9/2012).
[MANAGEMENT] This fast-paced podcast appearance with Chris Gammel on the "Amp Hour" touches on many of the finer points of life, including how to hide technical details from your boss, how to get a standard through the IEEE, and dealing with unwelcome co-workers.

Wire-Wrap. Newsletter *v2-8* (3/5/1998).
[WIRE WRAP] What are other simple ways of connecting two ICs together that are more robust than wire-wrap?

Words of Wisdom. HSSP Seminar (2015): 12.75.
[MANAGEMENT] Measure everything. Sit with your layout people. Make your hardware testable. (5 min.)

Words of Wisdom. EDN (4/3/2003).
[MANAGEMENT, TESTING] What instructions would you give to a development team working on a 10 Gb/s serial link?

Working with EMC Consultants. Newsletter *v5-10* (9/10/2002).
[EMC] The biggest EMC mistake you can make is the failure to get your consultant involved at a sufficiently early stage.

Working with People. HSNG Seminar (2015): 7.22-7.37.
[MANAGEMENT] Consultants. Special Assignments. Other Practical Advice. Thank You For Attending. (17 min.)

Yao! What a Handshake. EDN (2/7/2008).
[LEVEL TRANSLATION, TERMINATION] Making the output voltage equal VT is the easiest thing in the world for a driver. The terminating voltage is a "natural resting place". If you disconnect the driver, the load immediately relaxes, all by itself, to VT.

Your layout is skewed. EDN (4/18/2002).
[DIFFERENTIAL SIGNALING, SKEW] Chamfering or rounding of differential corners does not eliminate skew.

Z[min]. EDN (2/27/2008).
[LEVEL TRANSLATION, TERMINATION] Understanding Z[min], dear reader, is the secret to successful end-termination design.